

Compal Confidential

ISRAE LA-3711P Schematics Document

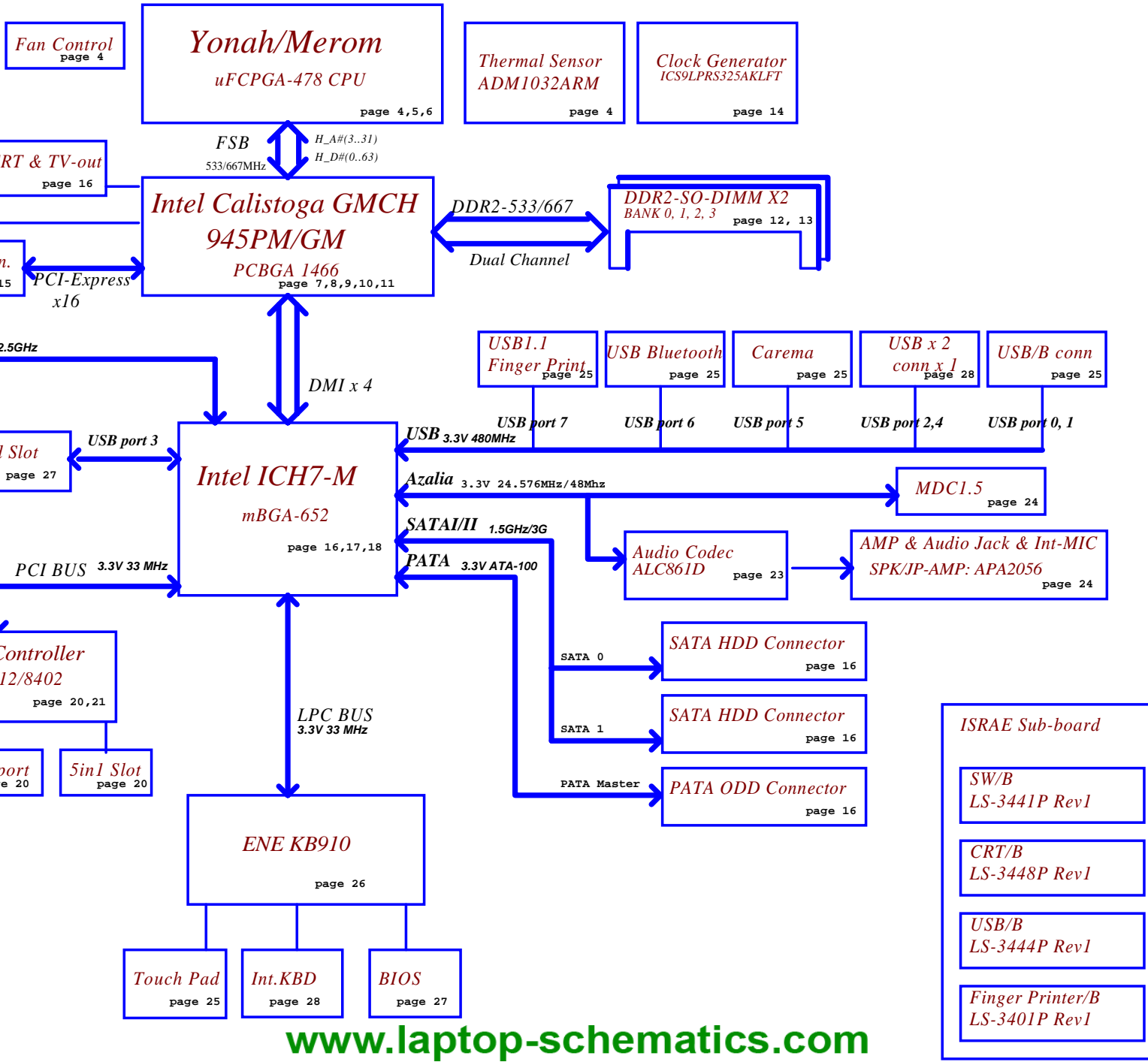
Intel Yonah/Merom with 945GM/943GML/940GML+ DDRII + ICH7M

2007-02-02

REV: 1.0

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				ISRAE M/B LA-3711P		
Date: Thursday, March 22, 2007				Sheet 1 of 39		



NVIDIA NB7P-GS
NB7M-SE
with 128/256
MB VRAM

10/100/1000 LAN
RTL8111B/RTL8101E
page 22

RJ45/11 CONN
page 22

LED
page 28

RTC CKT.
page 16

Power On/Off CKT.
page 28

DC/DC Interface CKT.
page 29

Power Circuit DC/DC
Page 30-36

CardBus Controller
TI PC18412/8402
page 20,21

Slot 0
page 21

1394 port
page 20

5in1 Slot
page 20

Touch Pad
page 25

Int.KBD
page 28

BIOS
page 27

ISRAE Sub-board

SW/B
LS-3441P Rev1

CRT/B
LS-3448P Rev1

USB/B
LS-3444P Rev1

Finger Printer/B
LS-3401P Rev1

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Date: Thursday, March 22, 2007			Sheet 2 of 39	

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	+VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD20	2	A,B,C
CARD BUS	D4	AD20	2	A,B,C
5IN1	D4	AD20	2	A,B,C

KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 1 0 1 1 X b
SM2 ADM0132	98H	1 0 1 1 0 0 X b
CPU THERMAL MONITOR		

ICH7-M SM Bus address

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	10 (10E)(10M)
1	10C
2	10G(10MG)
3	10GC
4	10J(10EJ) (10MJ)
5	10CJ
6	10G(10MG)J
7	10GC(10MGC)J

BTO Option Table

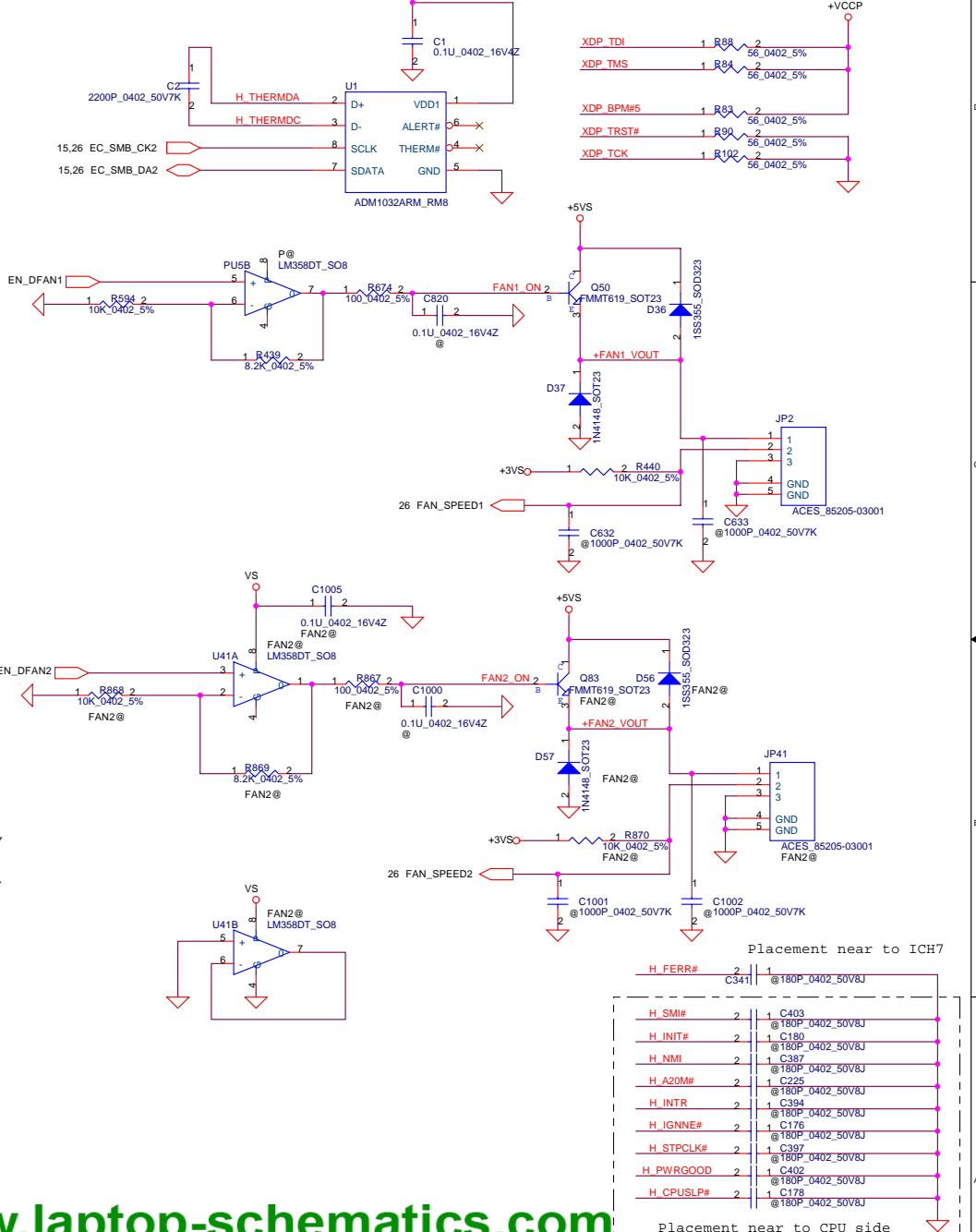
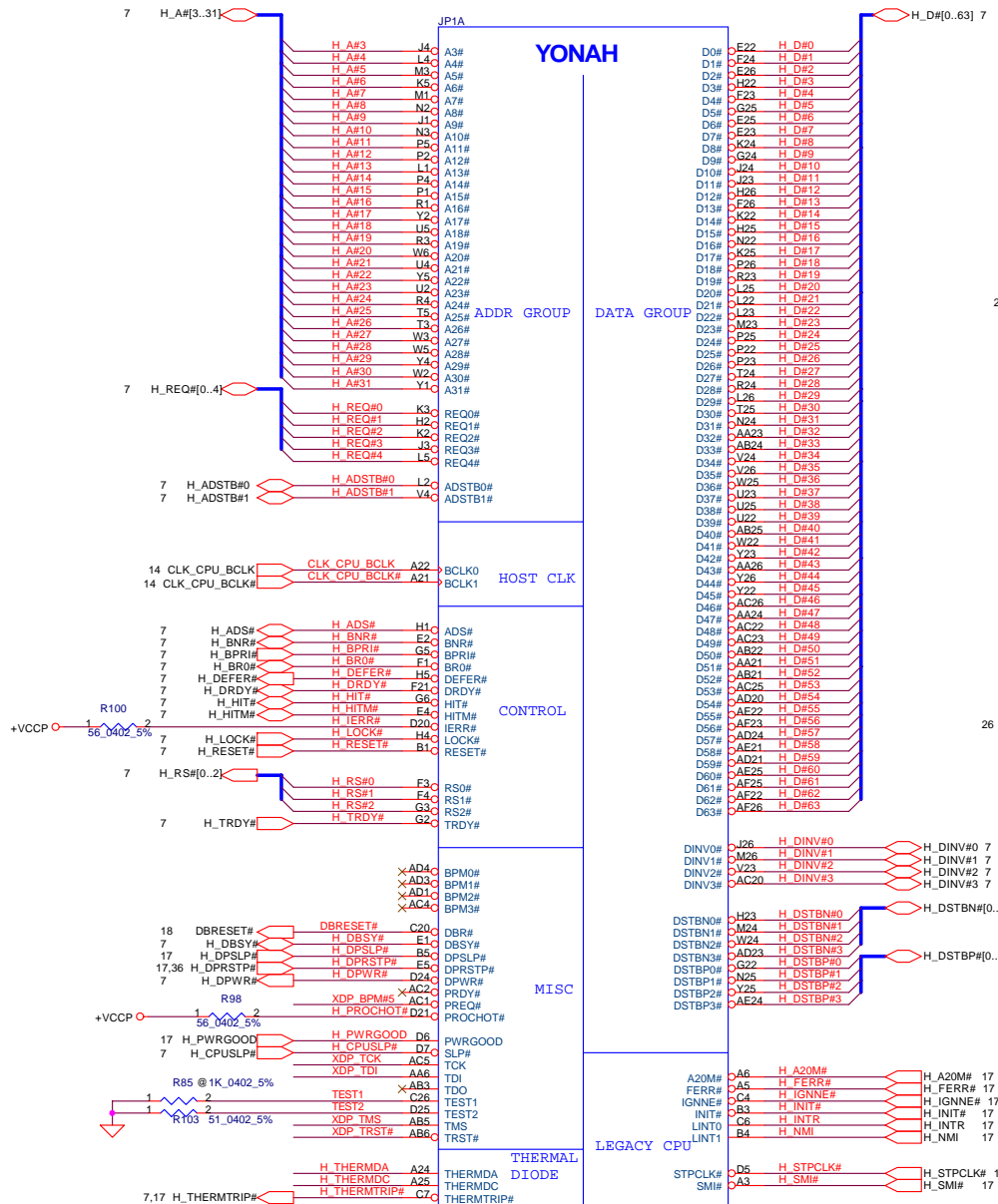
BTO Item	BOM Structure
45 level	45@
2ND HDD	2HDD@
LAN	100M@/1000M@
WLAN	KS@
MDC	MDC@
Blue tooth	BT@
Card ctrller	8412@/8402@/4512@
FINGER PRINT	FP@
5IN1	5IN1@, NON5IN1@
Express card	NEWCARD@
PCMCIA	PCMCIA@
Carema+MIC	CAREMA@
VGA FAN	FAN2@
CHIPSET (R3)	GMLR3@,GM@,ICH7R3@
change R3 to R1 for FRU	GMR3@,GM@,ICH7R3@
CIR	CIR@
Energy Star	ENG@

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				Size	Document Number
				ISRAE / M/B LA-3711P	
				Date:	Thursday, March 22, 2007
				Sheet	3 of 39
				Rev	1.0

Thermal Sensor ADM1032ARM

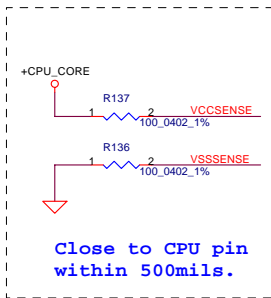
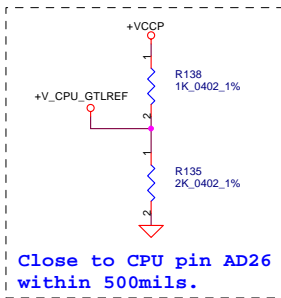
Place close to CPU within 500mil



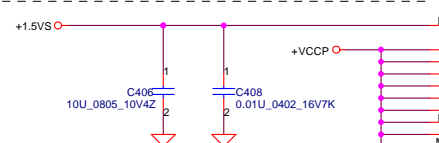
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil

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Size	Document Number	Rev	
	ISRAE MB LA-371IP	1.0	
Date:	Thursday, March 22, 2007	Sheet	4 of 39

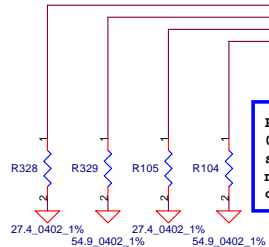


Length match within 25 mils
The trace width 18 mils space
7 mils

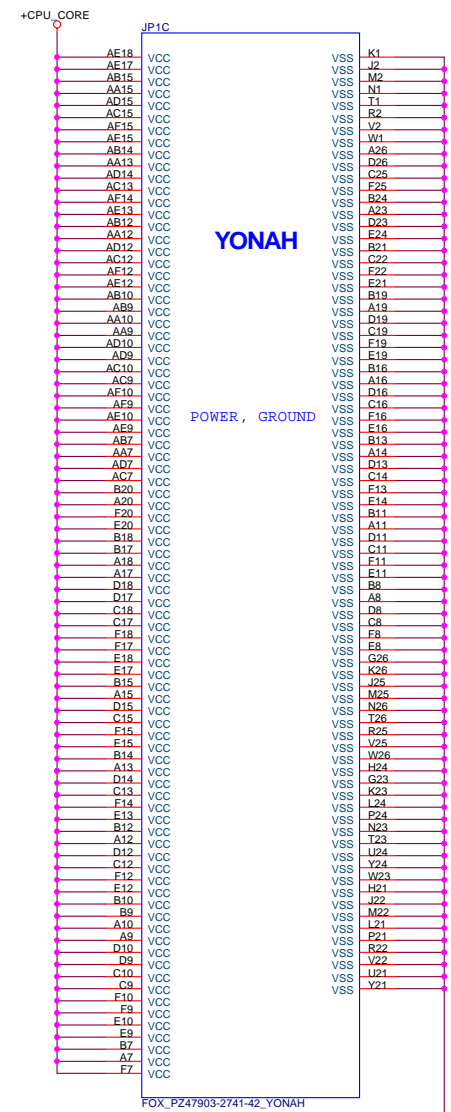
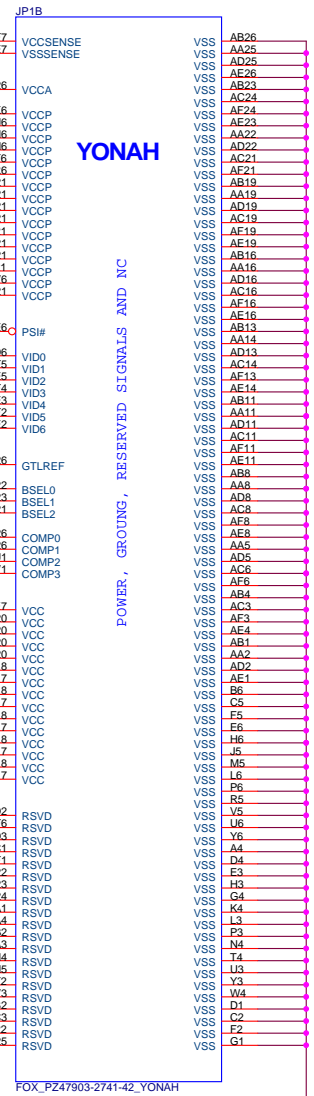


CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

CPU_VID0	CPU_VID1	CPU_VID2	CPU_VID3	CPU_VID4	CPU_VID5	CPU_VID6
AD6	AE6	AE5	AE4	AE3	AE2	AE2

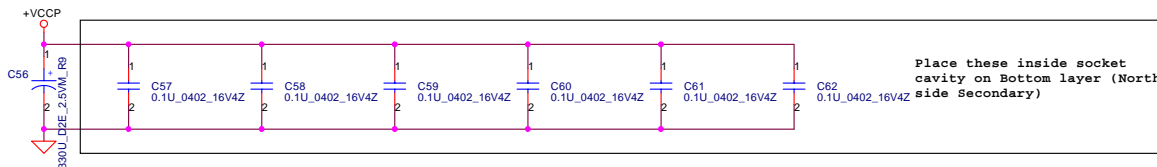
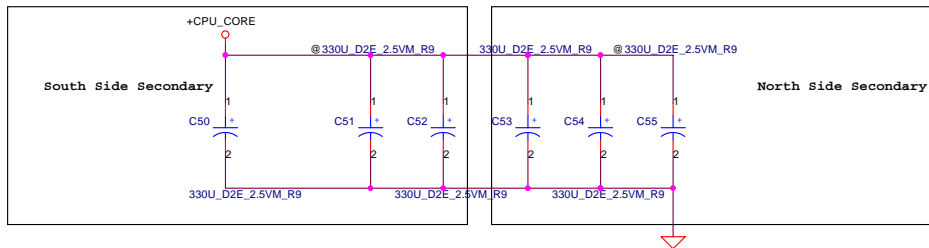
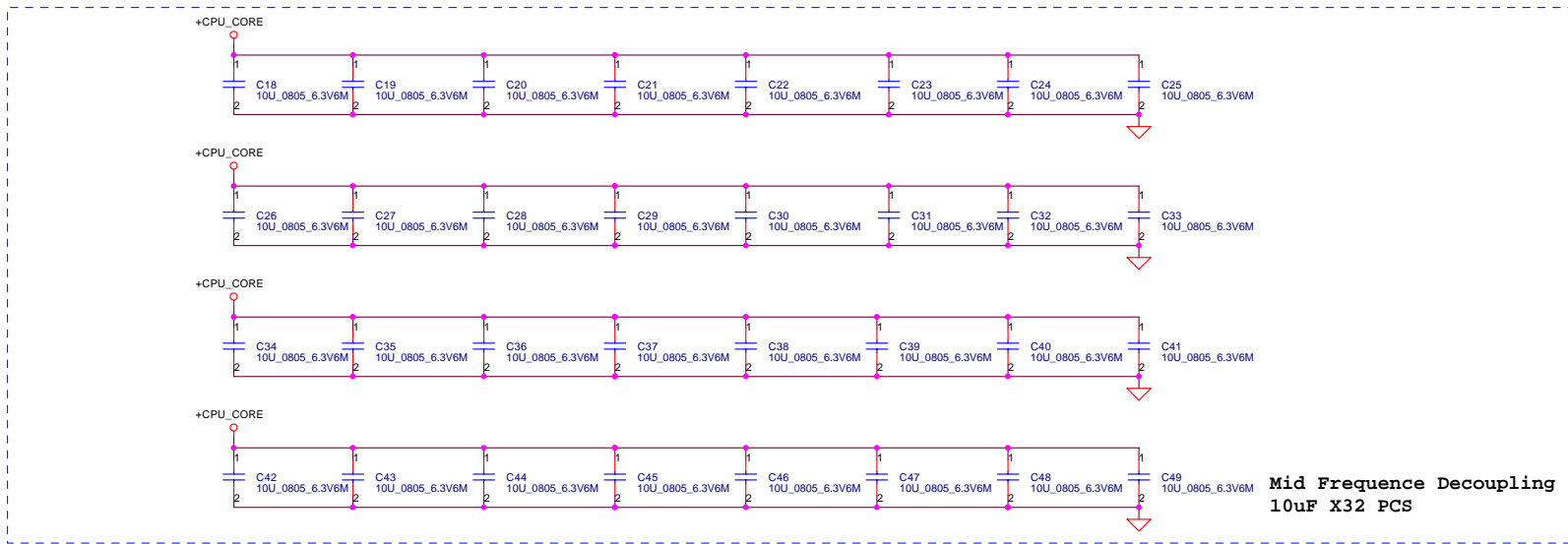


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.



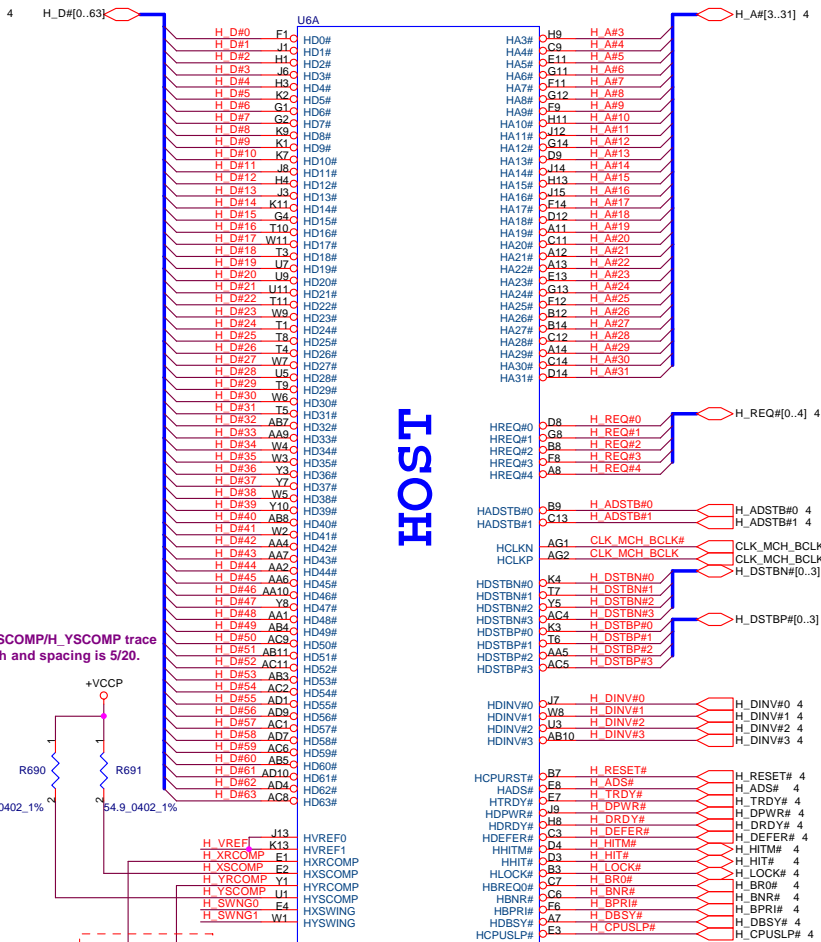
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Date:	Thursday, March 22, 2007	Sheet	5 of 39	



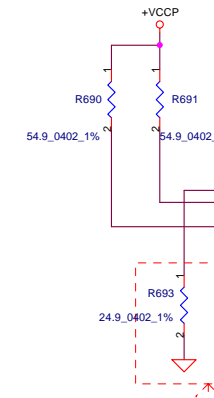
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				ISRAE M/B LA-371IP		1.0
Date: Thursday, March 22, 2007				Sheet	6	of 39

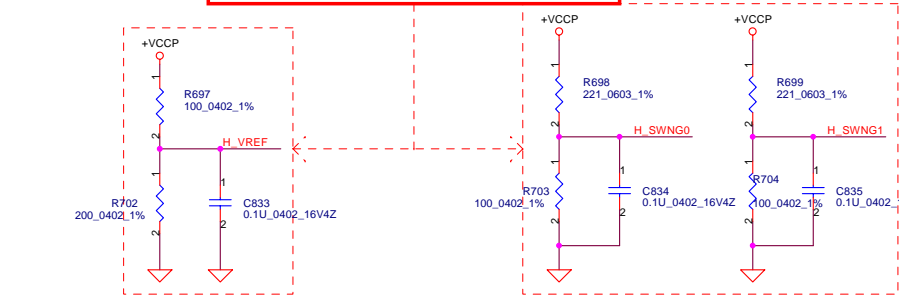


HOST

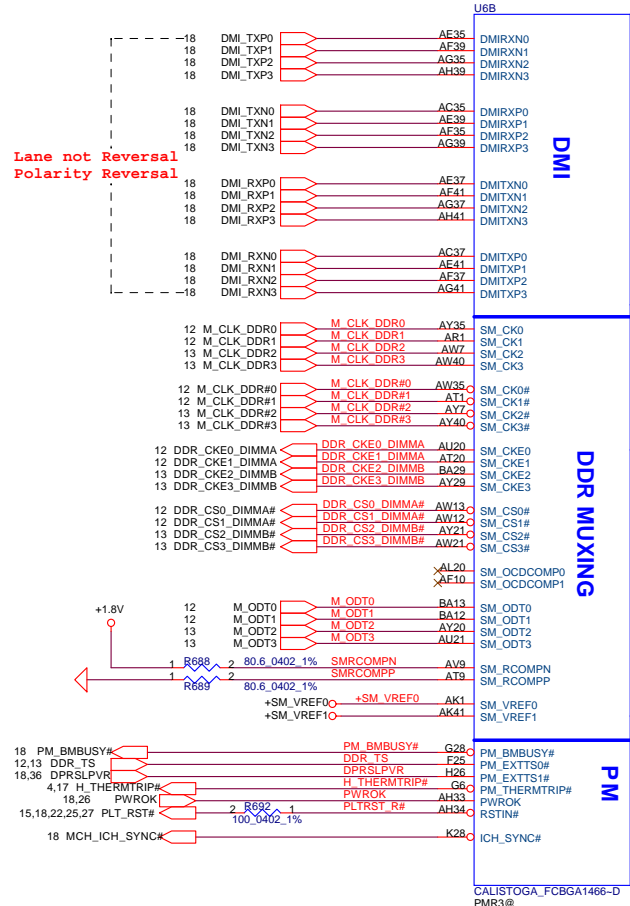
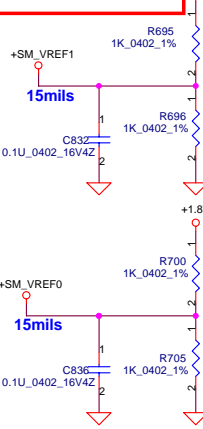
H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.



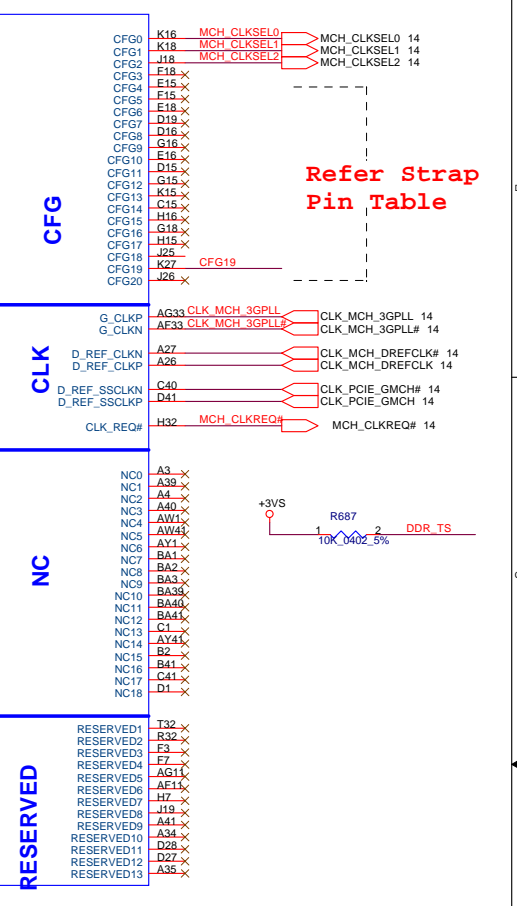
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.



Layout Note:
+SM_VREF0 & +SM_VREF1 trace width and spacing is 20/20.



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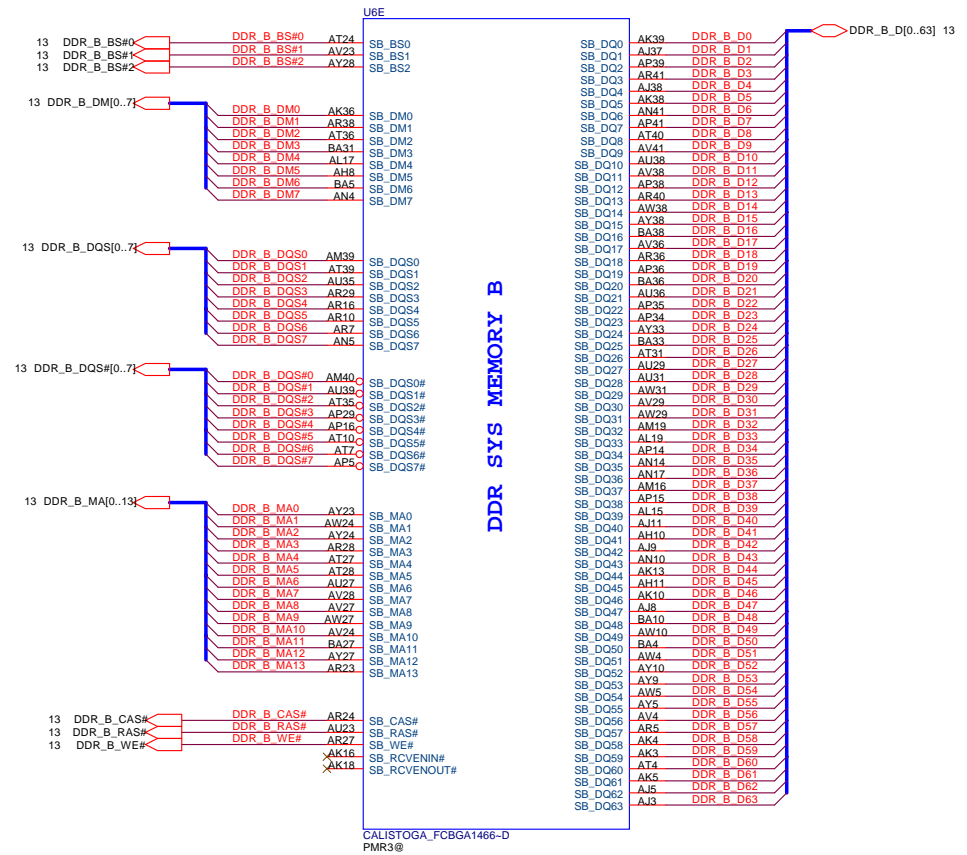
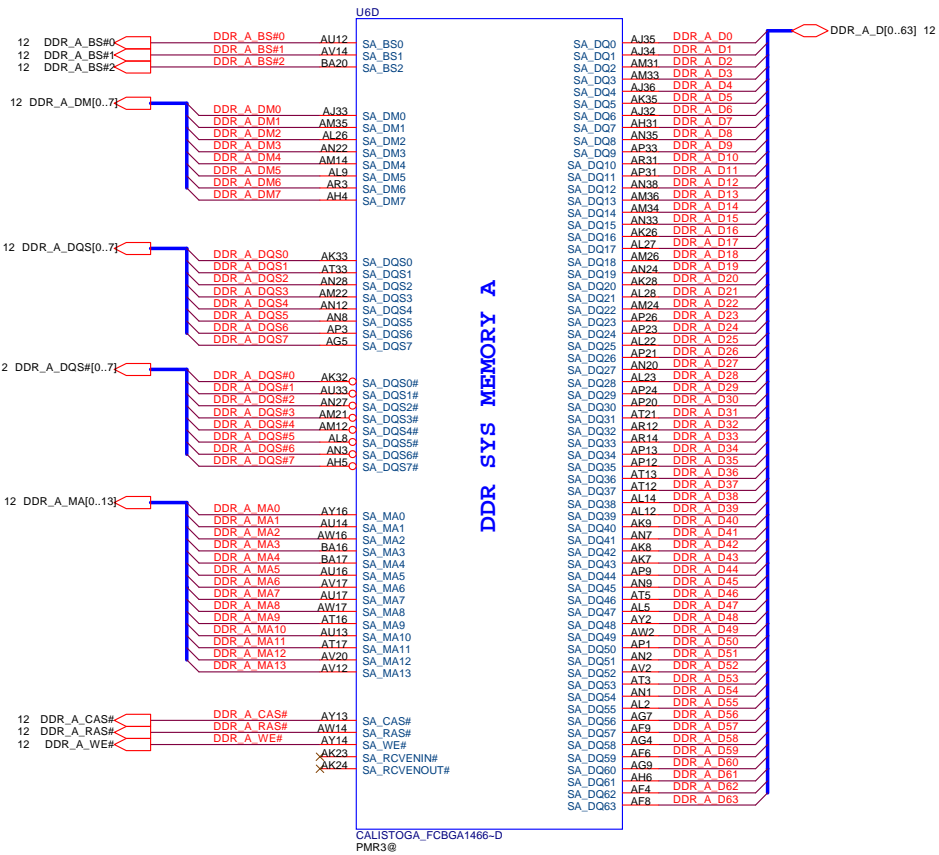


Strap Pin Table

CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

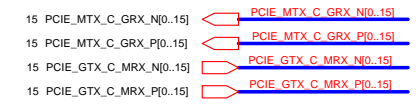
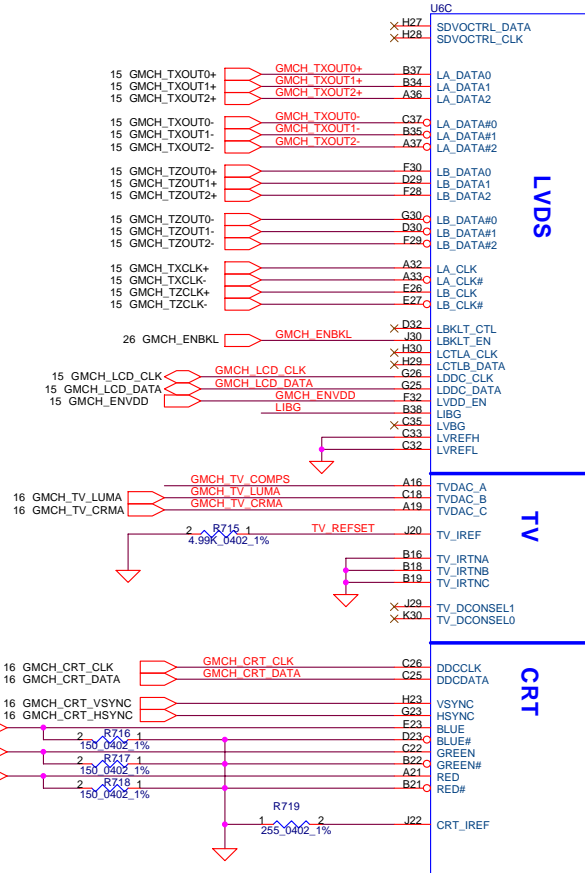
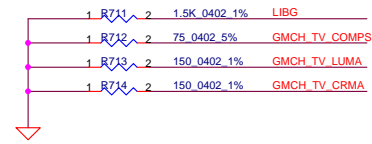
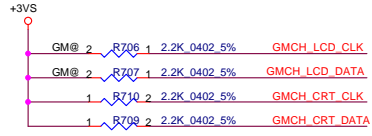
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 *1 = DMI x 4 (Default)
CFG7	0 = Reserved *1 = Mobile Yonah CPU (Default)
CFG9	0 = Lane Reversal Enable *1 = Normal Operation (Default)
CFG11	0 = Reserved *1 = Calistoga (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled *11 = Normal Operation (Default)
CFG16	0 = Dynamic ODT Disabled *1 = Dynamic ODT Enabled (Default)
CFG18	*0 = 1.05V (Default) 1 = 1.5V
CFG19	*0 = Normal Operation (Default) *1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	*0 = No SDVO Device Present (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	*0 = Only PCIE or SDVO is operational. (Default) 1 = PCIE/SDVO are operating simu.

Title		Compal Electronics, Inc.	
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Size	Document Number	ISRAE M/B LA-3711P	Rev 1.0
Date:	Thursday, March 22, 2007	Sheet 7	of 39

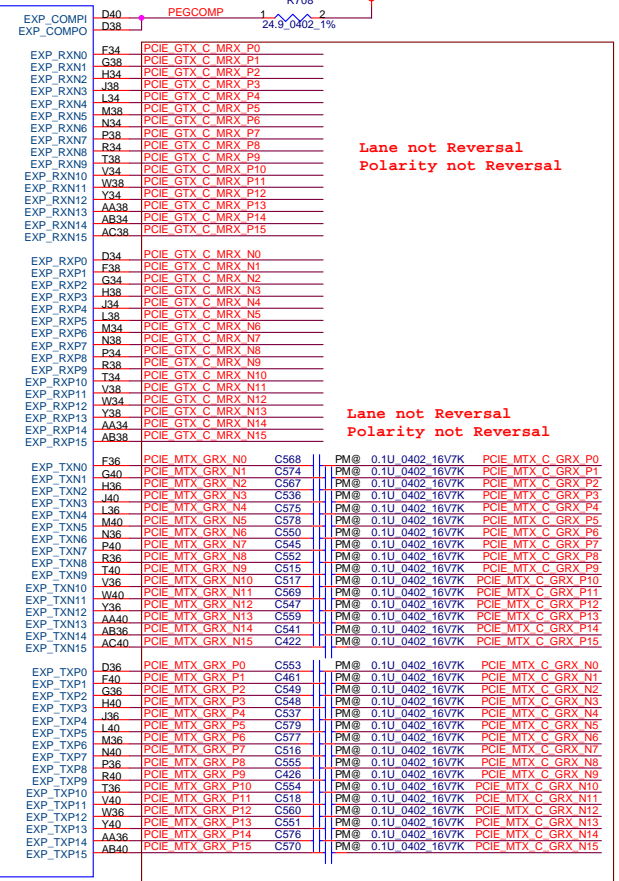


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Size	Document Number	Date		Rev	
	ISRAE MB LA-371IP	Thursday, March 22, 2007	Sheet 8 of 39	1.0	



PEGCOMP trace width and spacing is 18/25 mils.



Lane not Reversal
Polarity not Reversal

Lane not Reversal
Polarity not Reversal

PCI-EXPRESS GRAPHICS

LVDS

TV

CRT

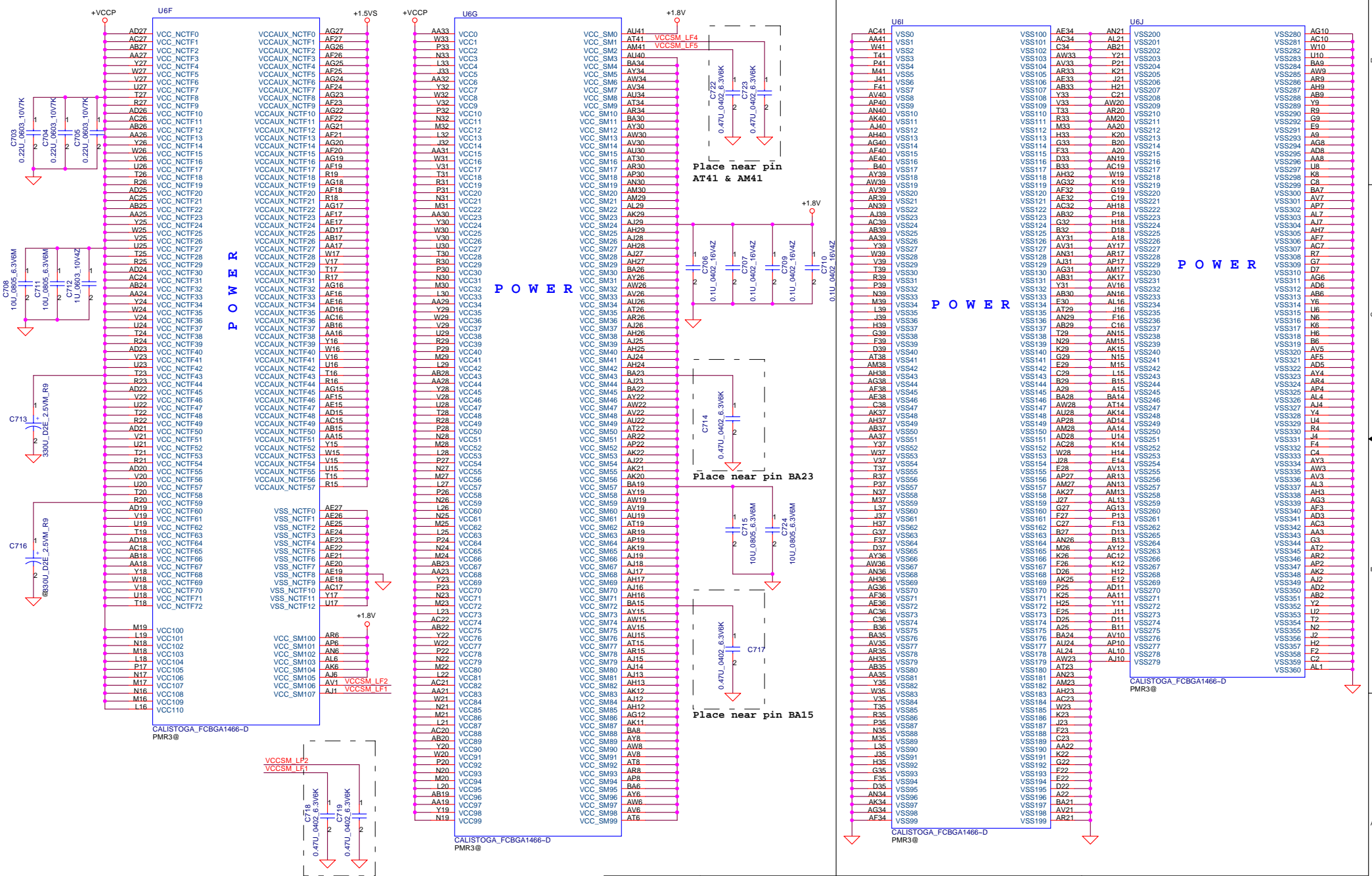
CALISTOGA_FCBGA1466-D
PMR3@

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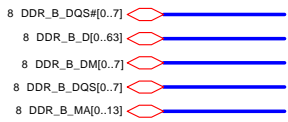
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				ISRAE M/B LA-3711P	Rev 1.0
				Date: Thursday, March 22, 2007	Sheet 9 of 39

POWER

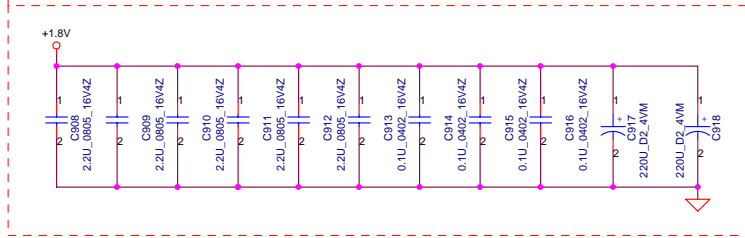
GND



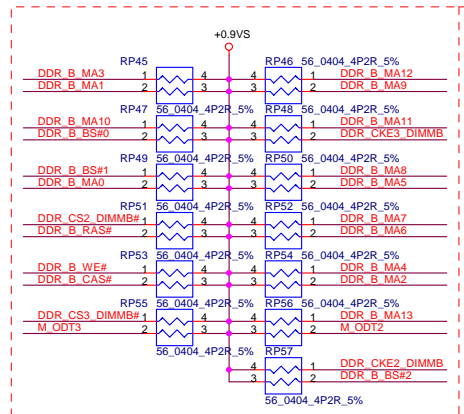
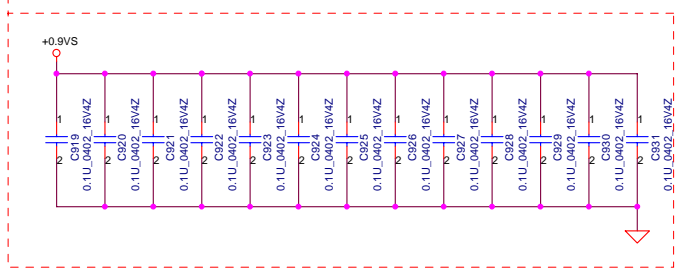
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				ISRAE MB LA-371IP	
Date:	Thursday, March 22, 2007	Sheet	11	of	39



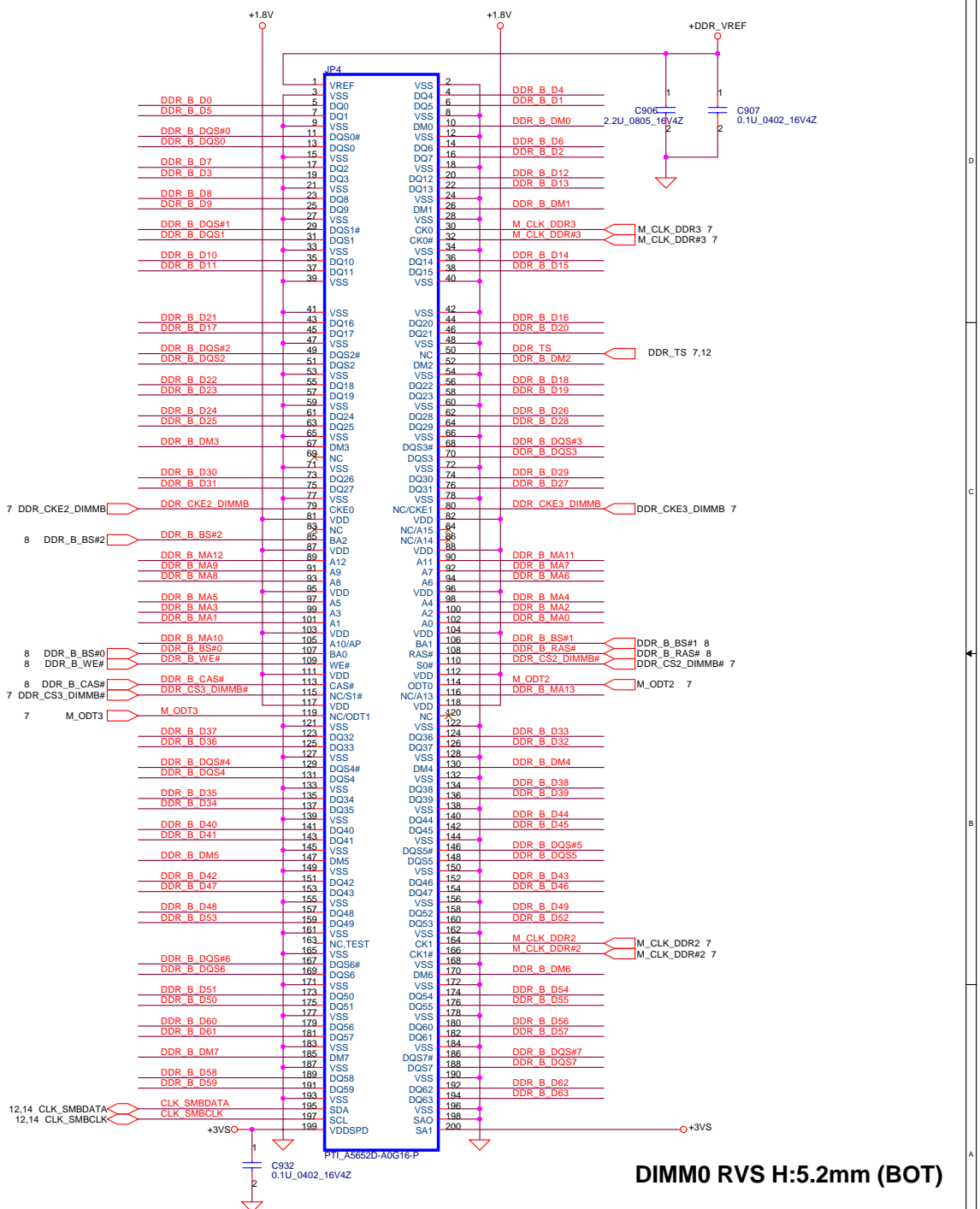
Layout Note:
Place near JP26



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

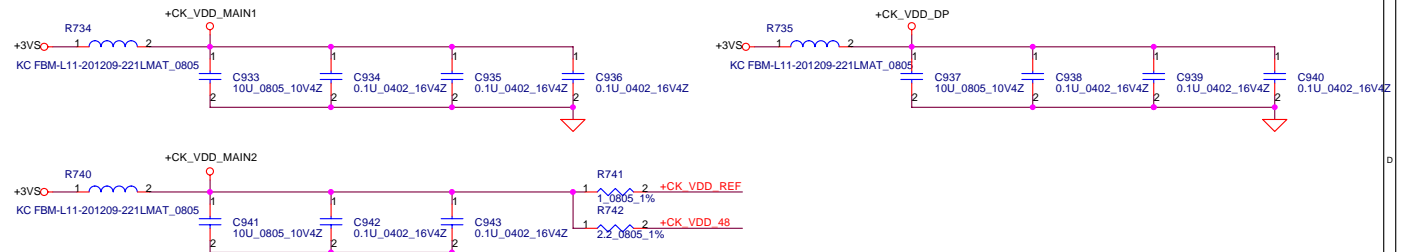
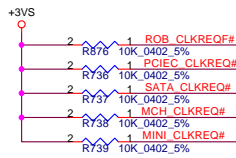


Layout Note:
Place these resistor closely JP26, all trace length Max=1.5"



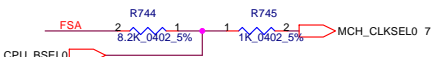
DIMM0 RVS H:5.2mm (BOT)

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				DDRII-SODIMM SLOT2	
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				ISRAE MB LA-371IP	
Date:	Thursday, March 22, 2007	Sheet	13	of	39

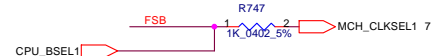


FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

FSA

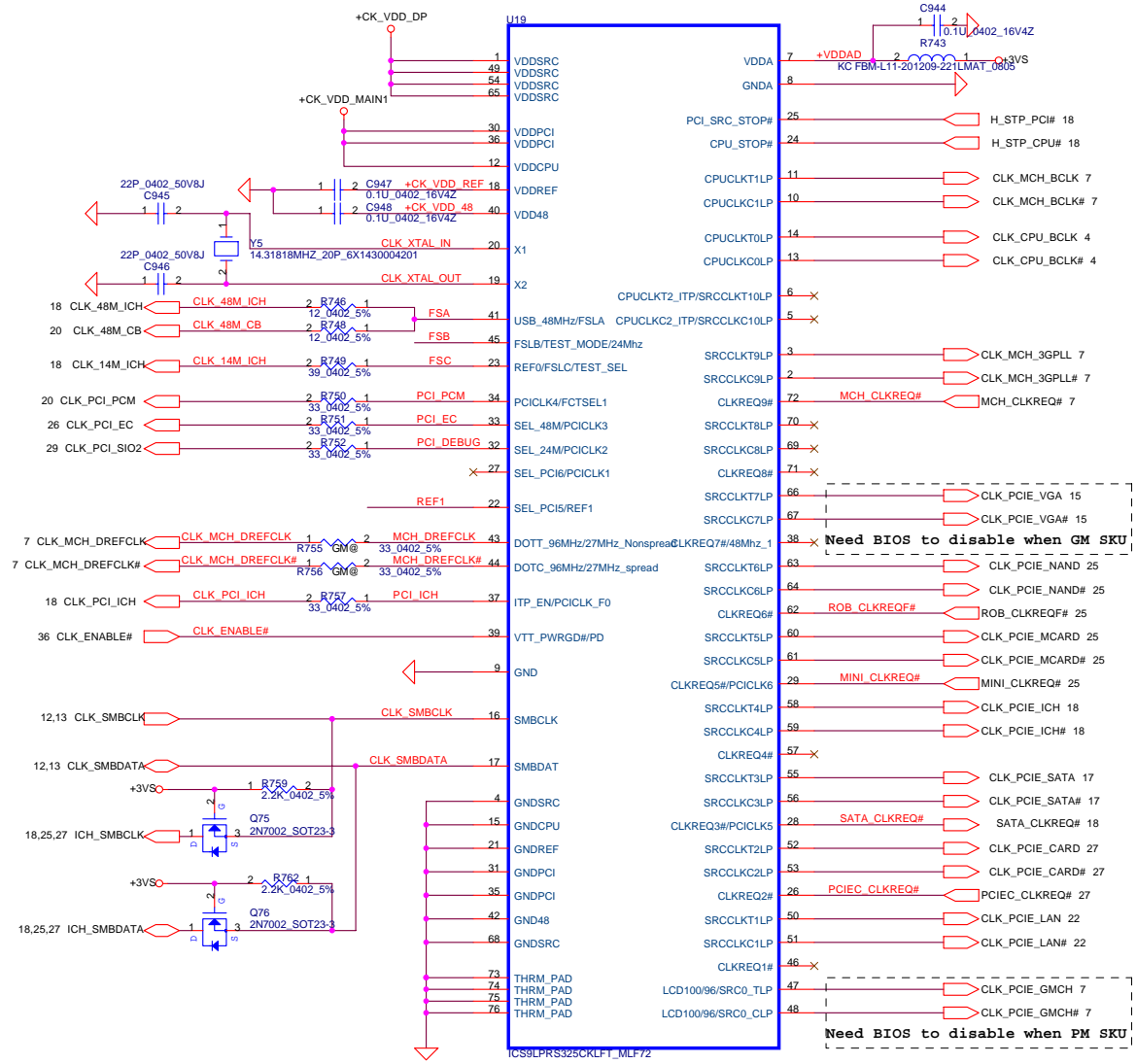
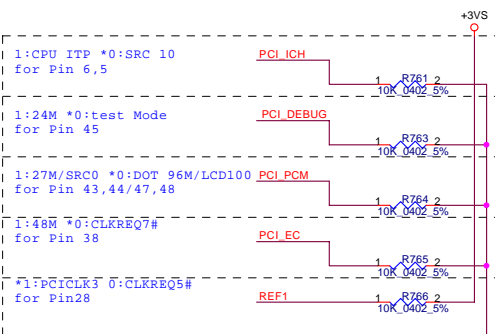
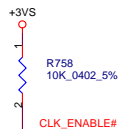
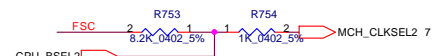


FSB



FSC

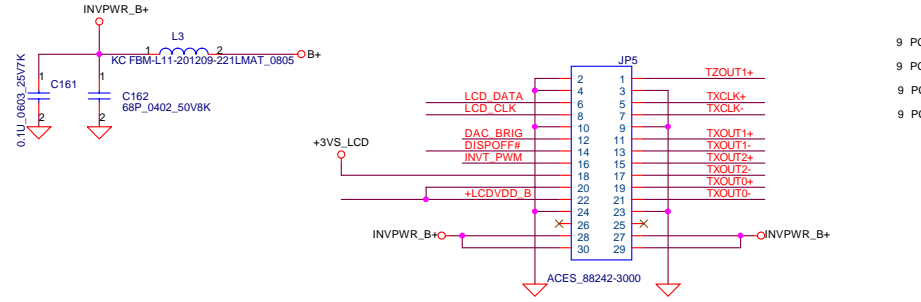
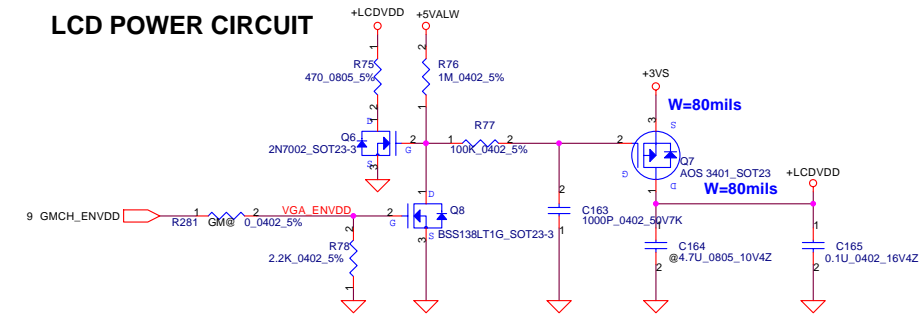
(Fixed at low)



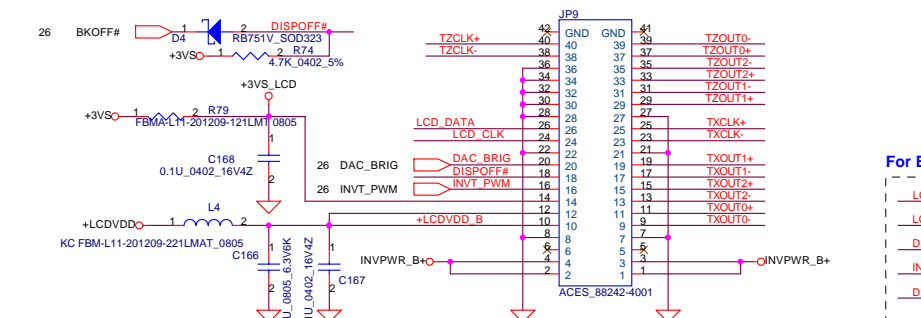
Security Classification			Compal Secret Data			Title		
Issued Date	2006/11/05	Deciphered Date	2009/11/05	Compal Electronics, Inc.			Clock generator	
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							ISRAE M/B LA-3711P	1.0
						Date:	Thursday, March 22, 2007	Sheet 14 of 39

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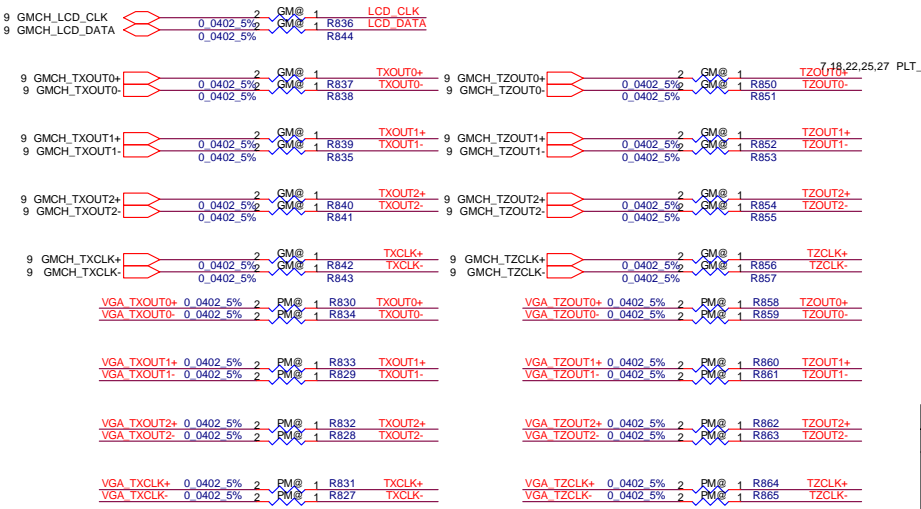
LCD POWER CIRCUIT



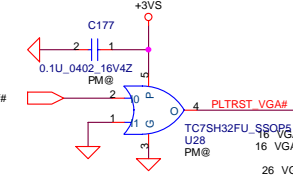
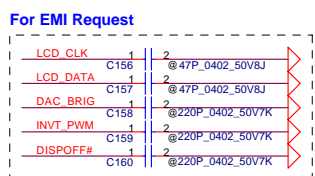
LCD/PANEL BD. Conn.



ALL R CLOSE LVDS CONNECTOR



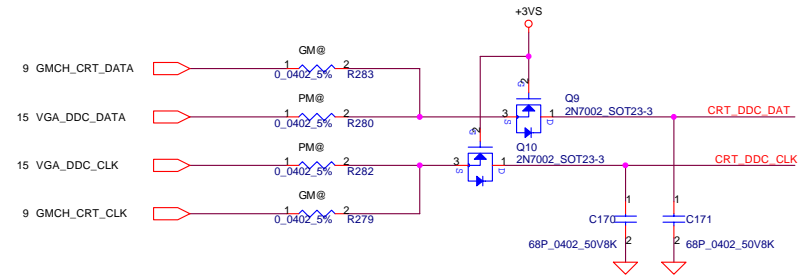
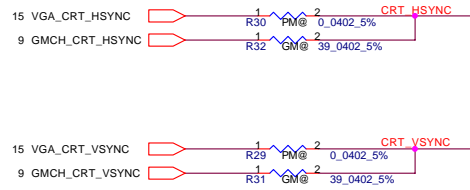
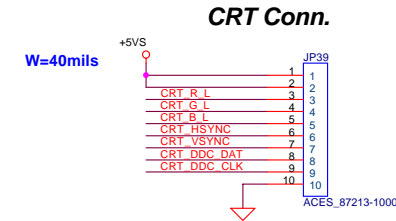
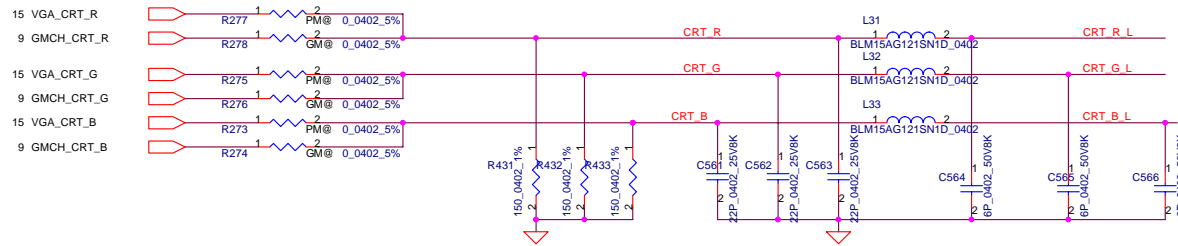
VGA BOARD Conn. VGA BOARD Conn.



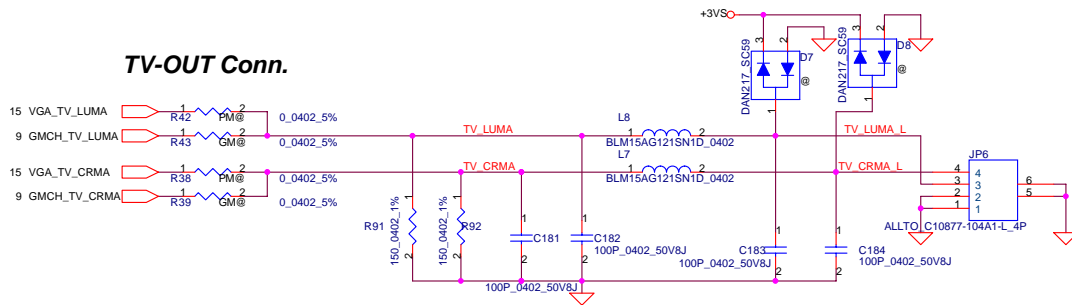
Security Classification	Compal Secret Data		Title	
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Compal Electronics, Inc.
VGA CONN				
Size	Document Number	ISRAE M/B LA-3711P		Rev 1.0
Date:	Thursday, March 22, 2007	Sheet	15	of 39

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CRT CONNECTOR



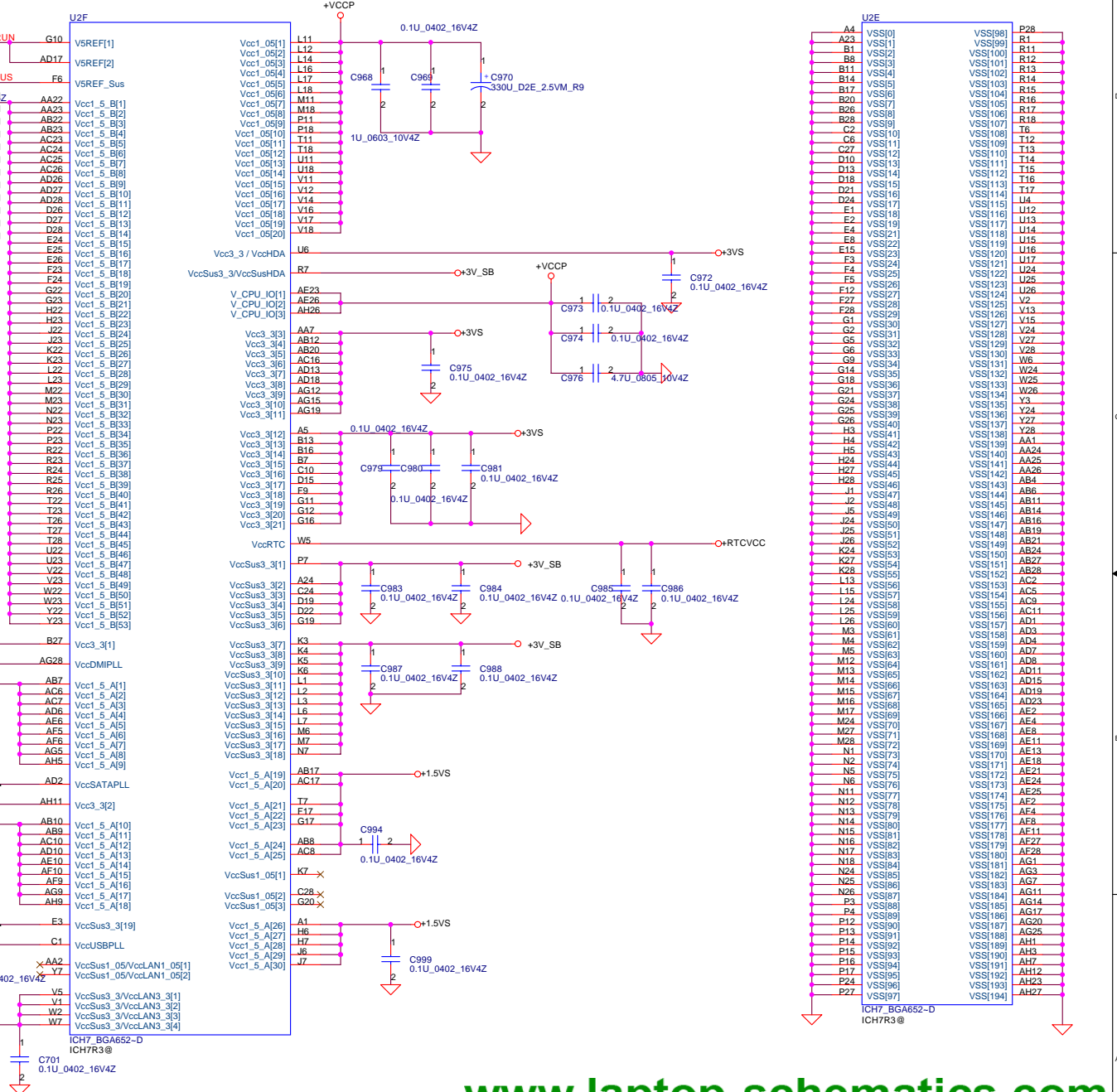
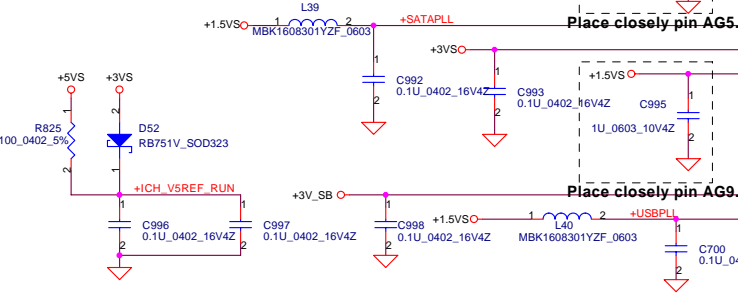
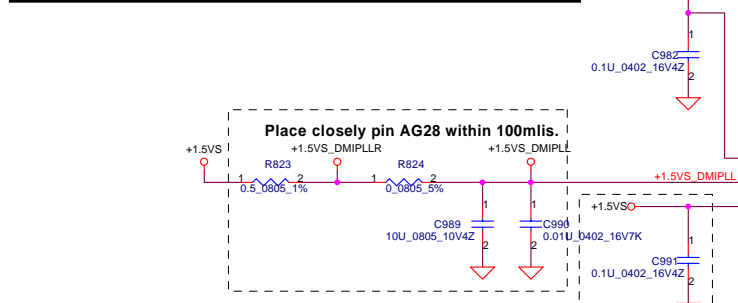
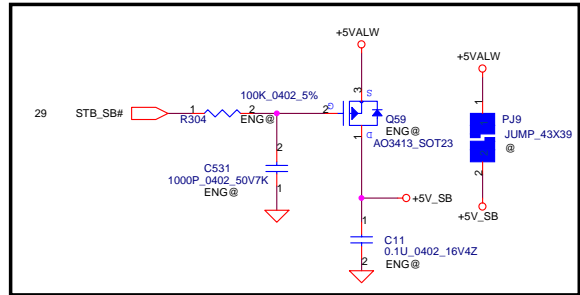
TV-OUT Conn.



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Size			Document Number	Rev
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Date:		Thursday, March 22, 2007	Sheet	16 of 39

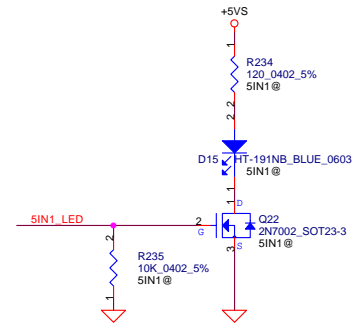
For Energy Star



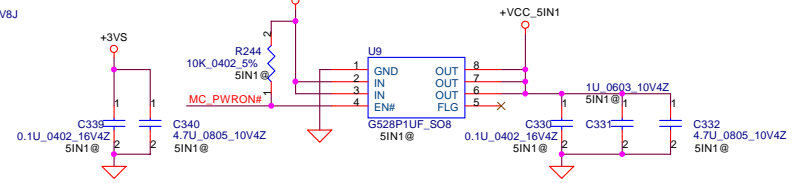
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				ISRAE MB LA-371IP	
Date:	Thursday, March 22, 2007	Sheet	19	of	39

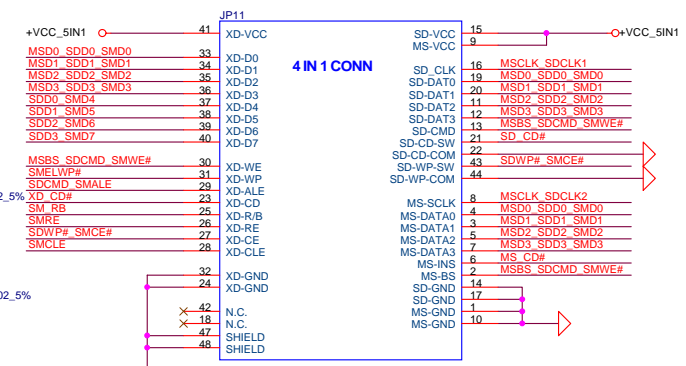
4 IN 1 LED



4 In 1 Card Power Switch



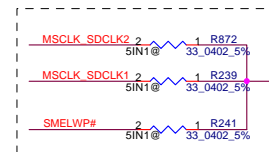
4 in 1 CardReader Conn.



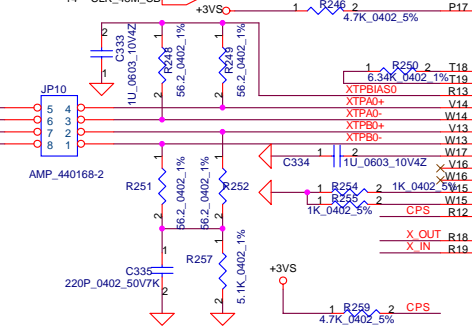
Bottom Side, Normal Insertion

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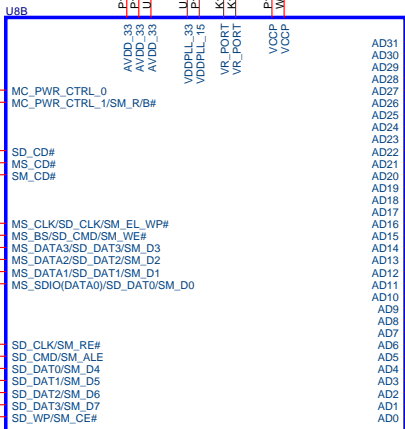
18 PCI_AD[0..31] <-> PCI_AD[0..31]
18 PCI_CBE[0..3] <-> PCI_CBE[0..3]



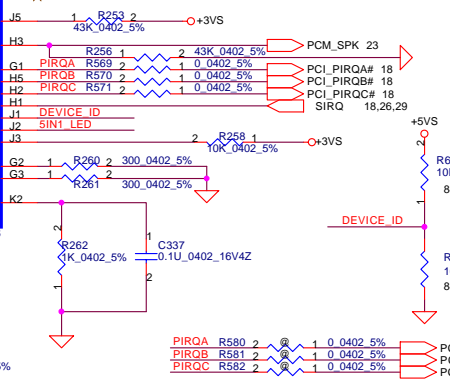
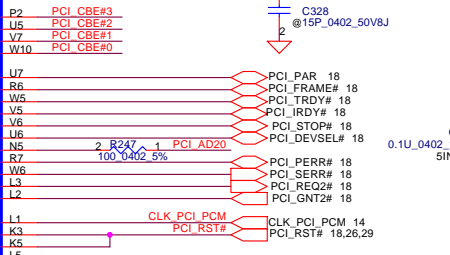
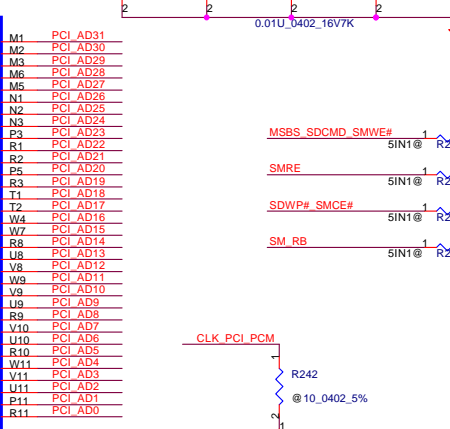
place near Chip 8412



CLOSE TO CHIP



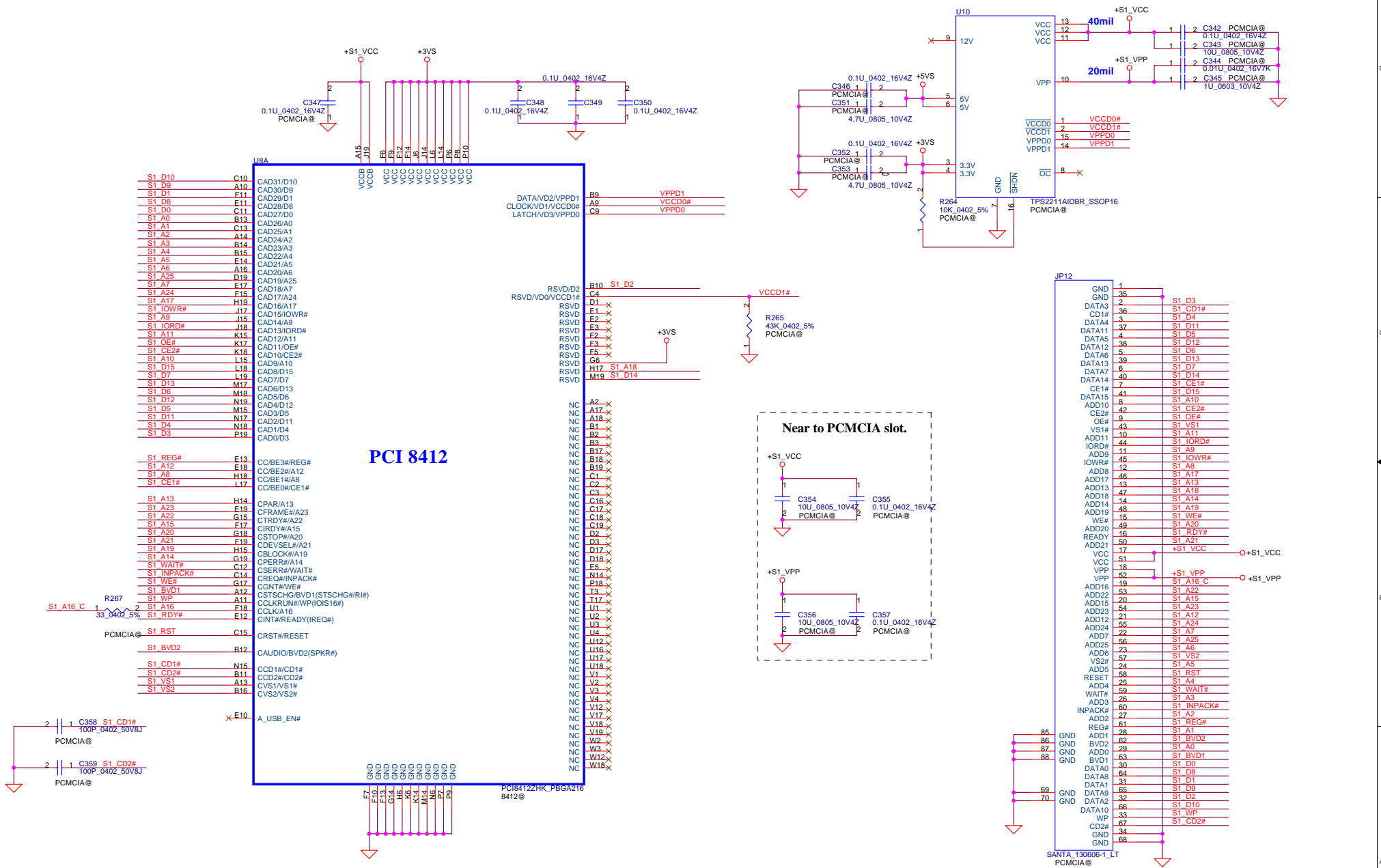
PCI8412



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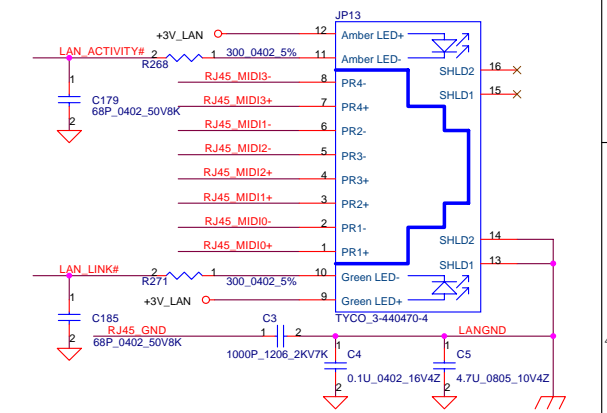
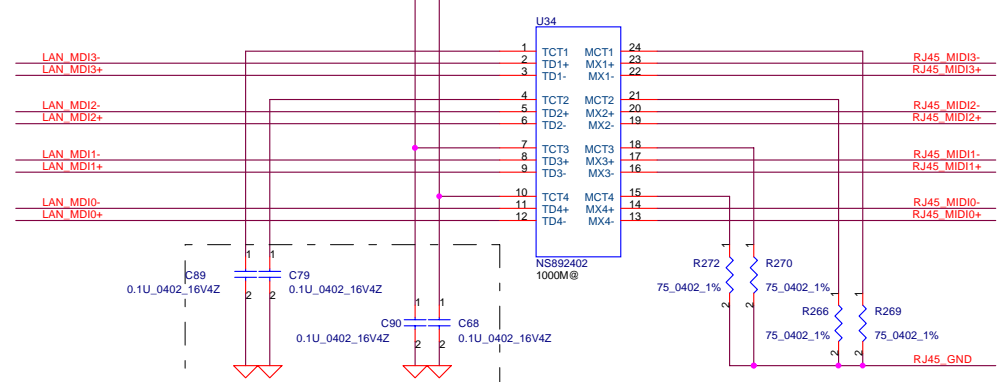
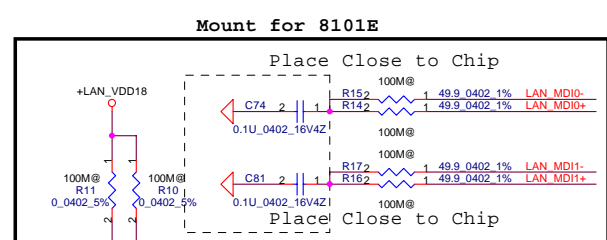
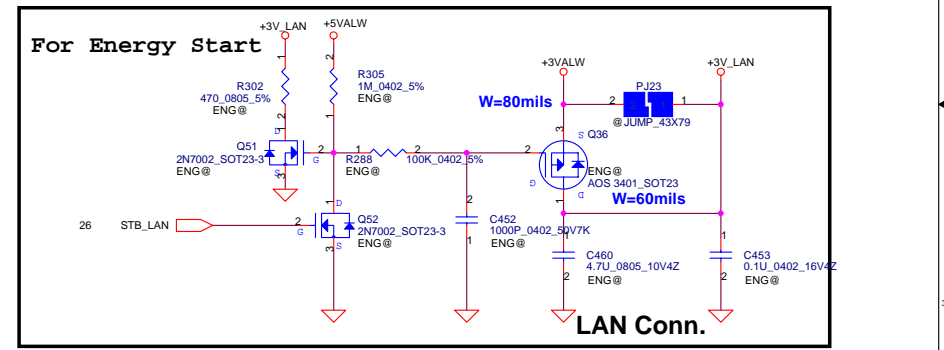
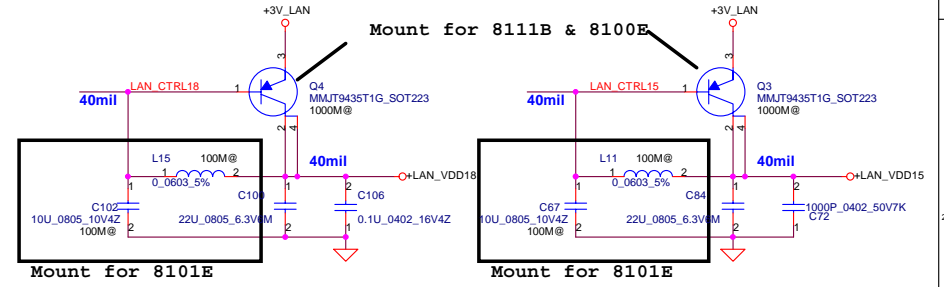
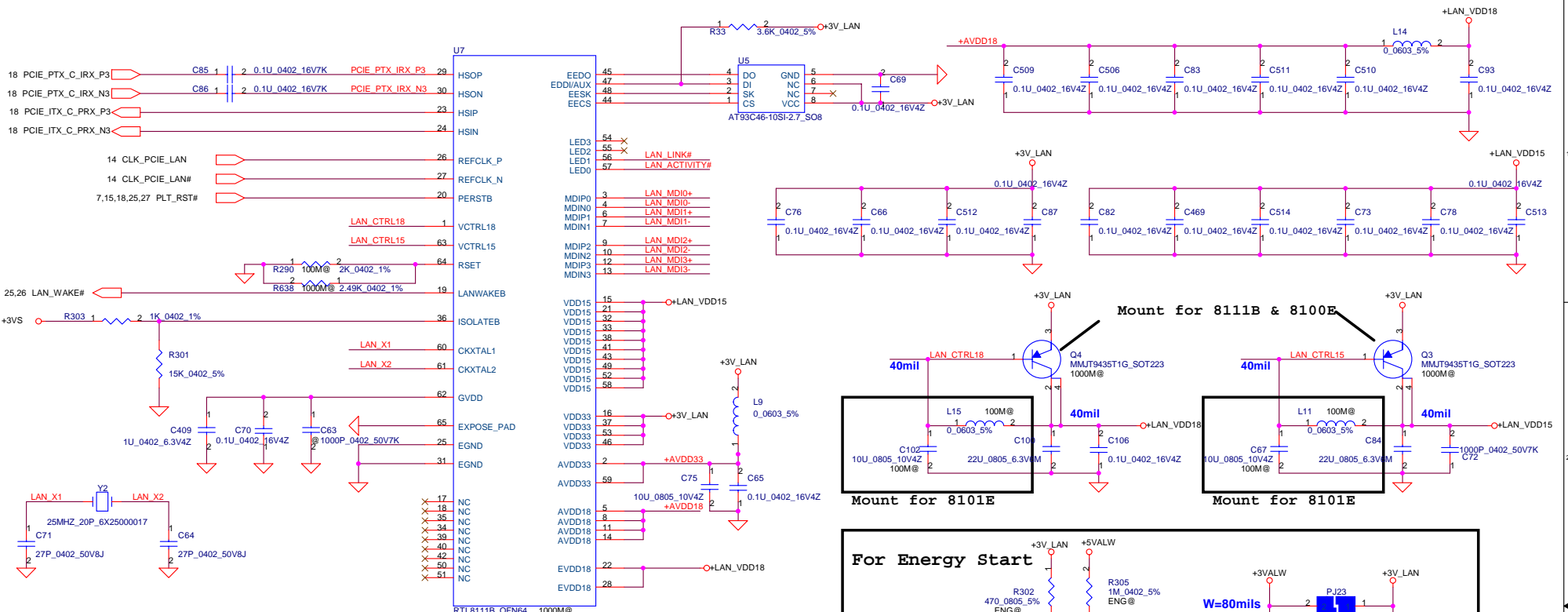
Compal Electronics, Inc.		
Title		
PCI8412/PCI1394 CONN/CARD SLOT		
Size	Document Number	Rev
Custom	ISRAE M/B LA-3711P	1.0
Date:	Thursday, March 22, 2007	Sheet 20 of 39

CardBus Power Switch



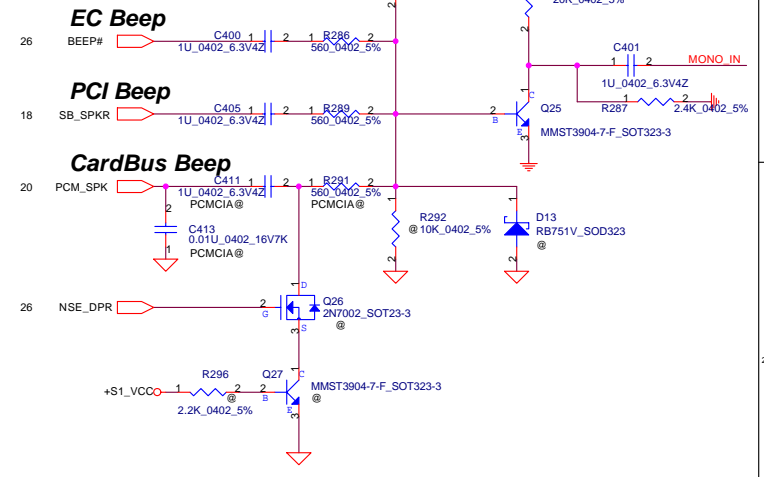
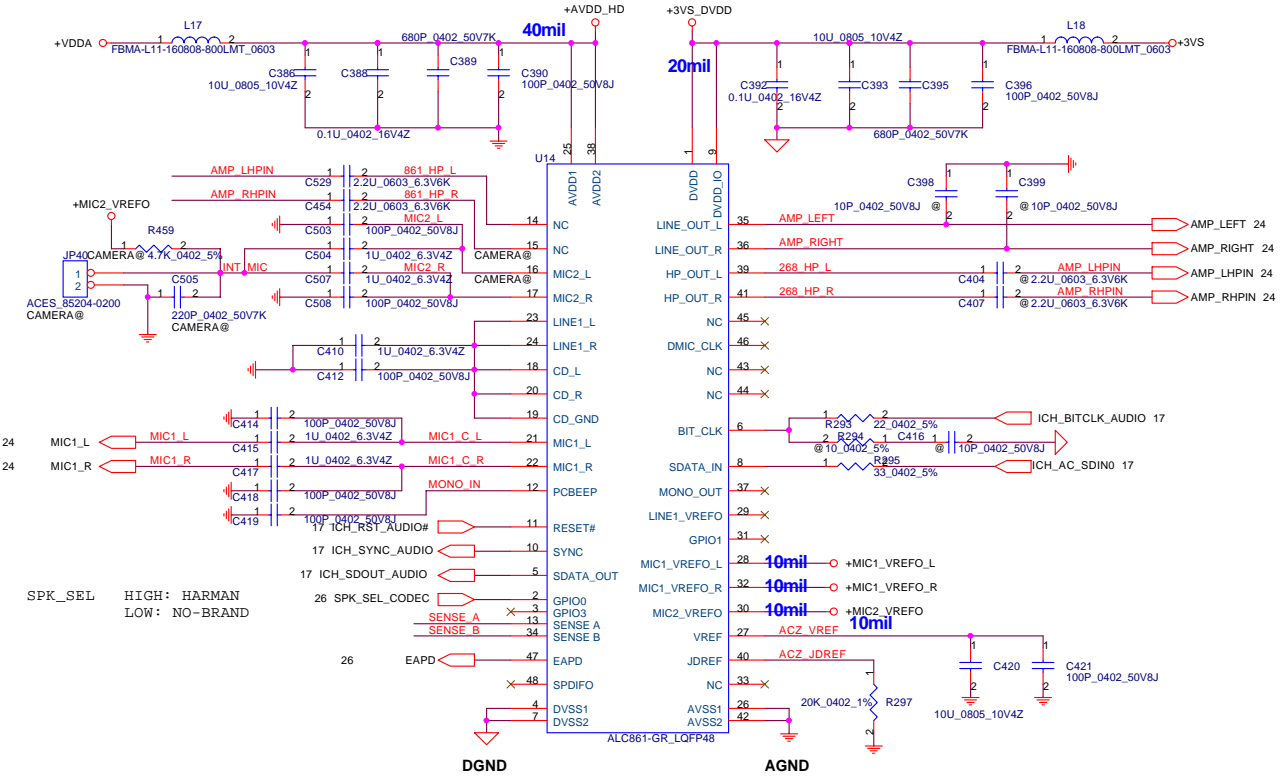
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	PCI7412/CB/CB SLOT	
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Date:	Thursday, March 22, 2007	Sheet	21 of 39	Rev	1.0



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				Customer	SRAE M/B LA-3711P
				Date:	Thursday, March 22, 2007
				Sheet	22 of 39

HD Audio Codec

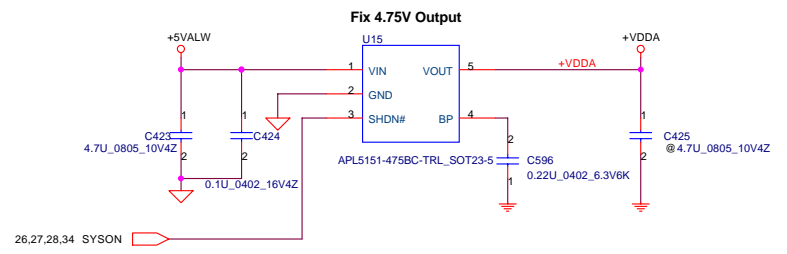


SPK_SEL HIGH: HARMAN
LOW: NO-BRAND

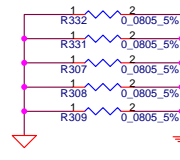
DGND

AGND

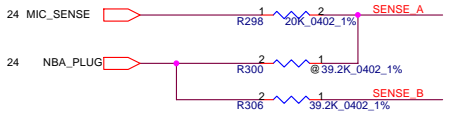
Regulator for CODEC



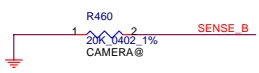
Moat Bridge



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

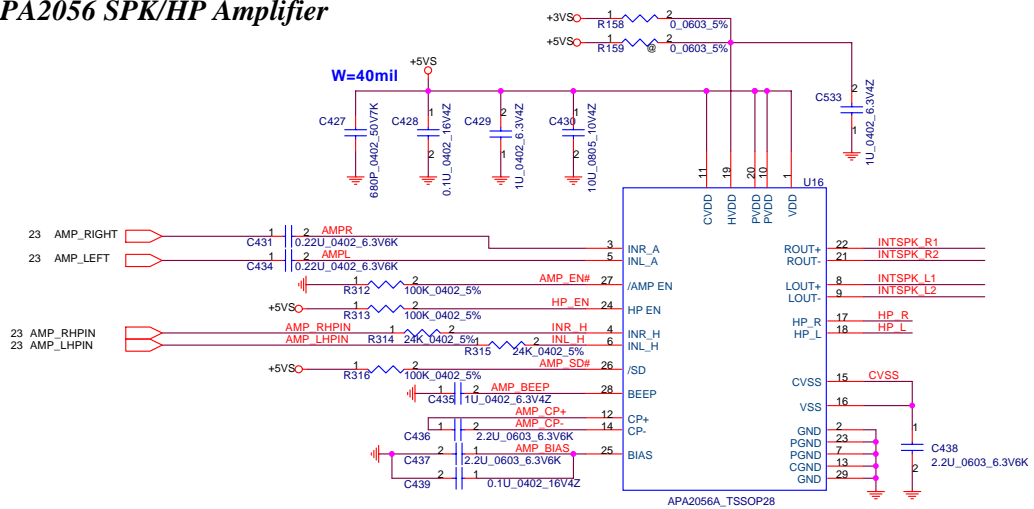


SENSE FOR Int. Mic.

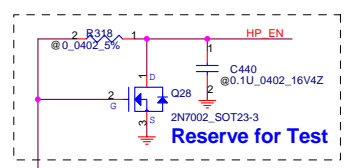


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				Custom	ISRAE M/B LA-3711P	1.0
				Date:	Thursday, March 22, 2007	Sheet 23 of 39

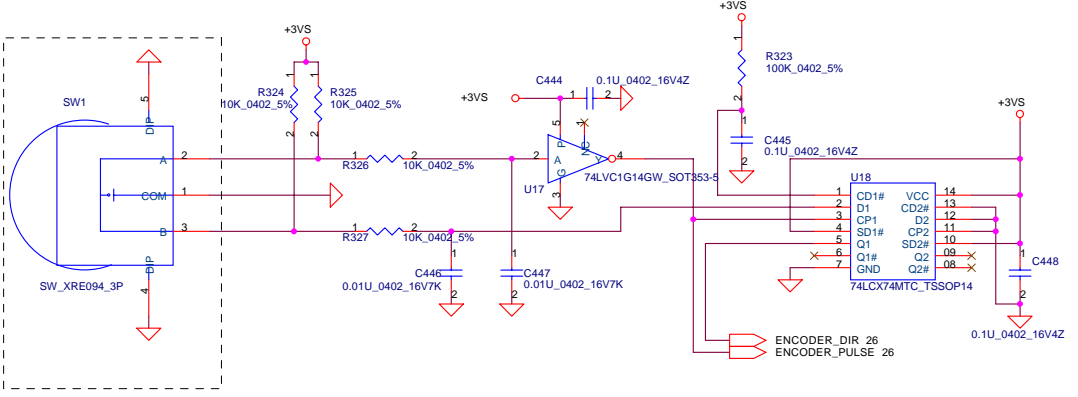
APA2056 SPK/HP Amplifier



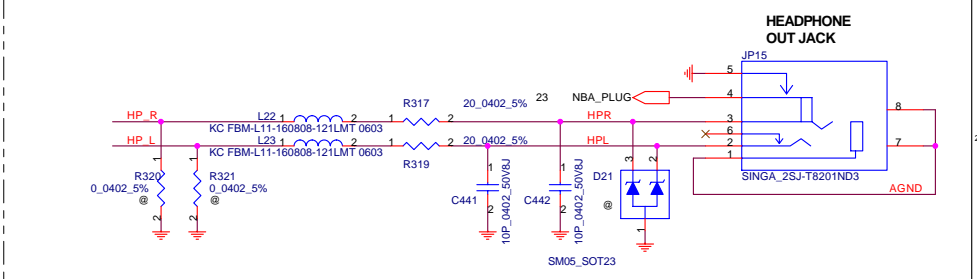
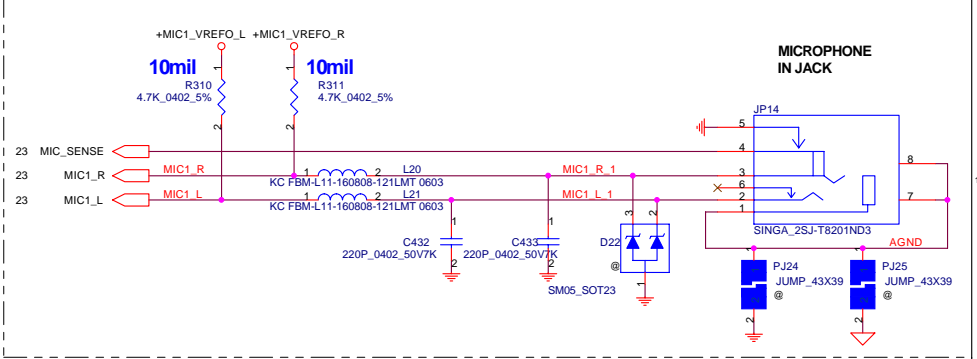
IN_A Gain = 10dB (Internal Speaker)
IN_H Gain = 0dB (Headphone)



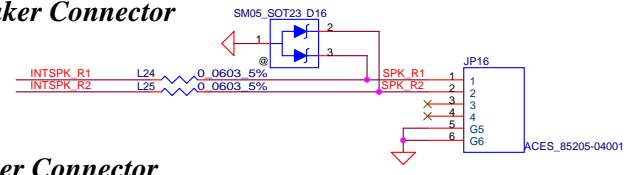
Volume Control



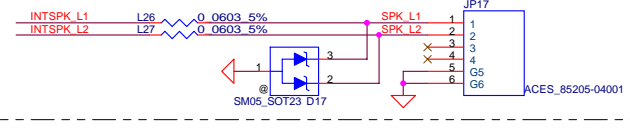
MP need to change P/N DEB00000600



Right Speaker Connector

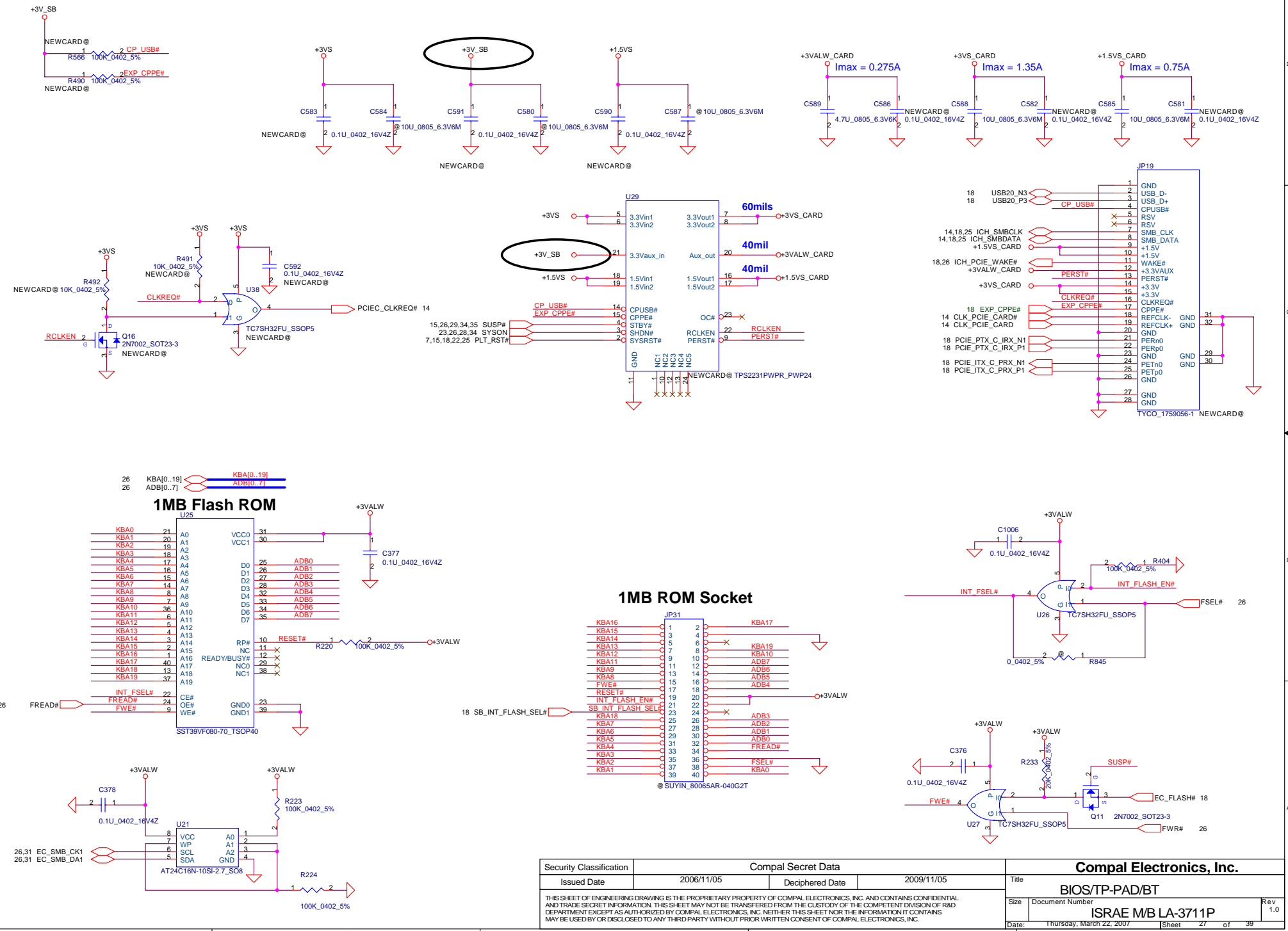


Left Speaker Connector



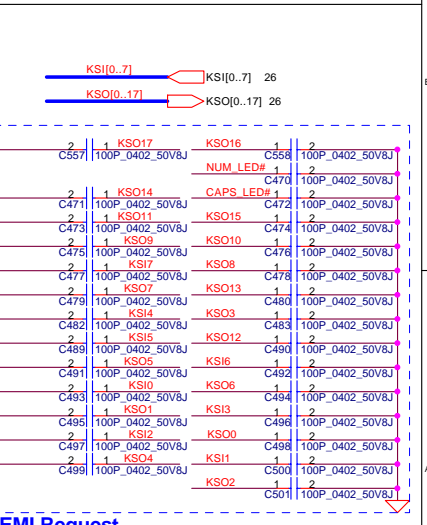
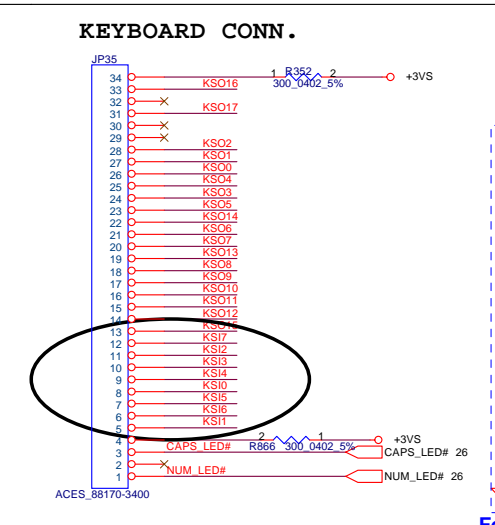
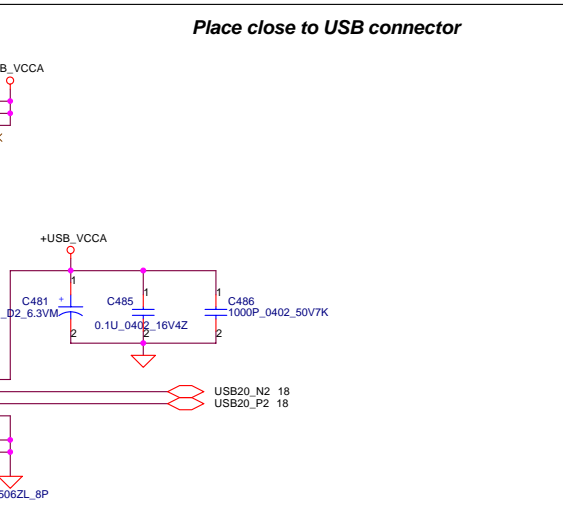
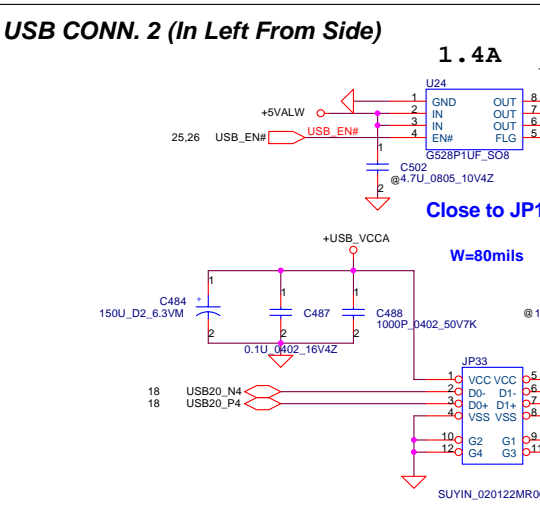
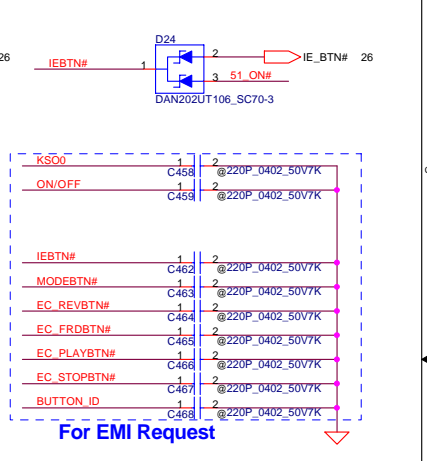
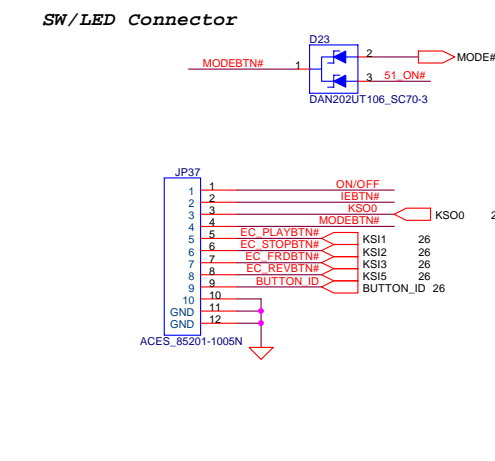
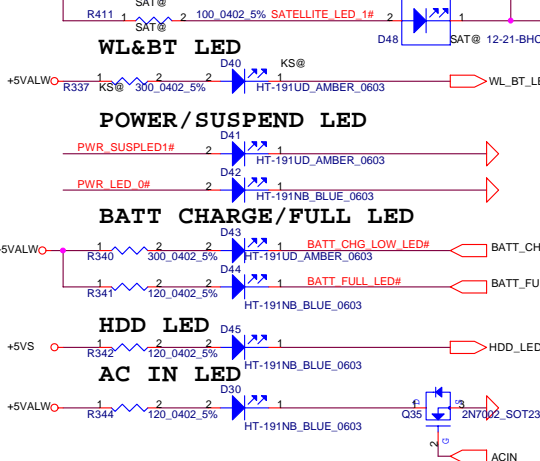
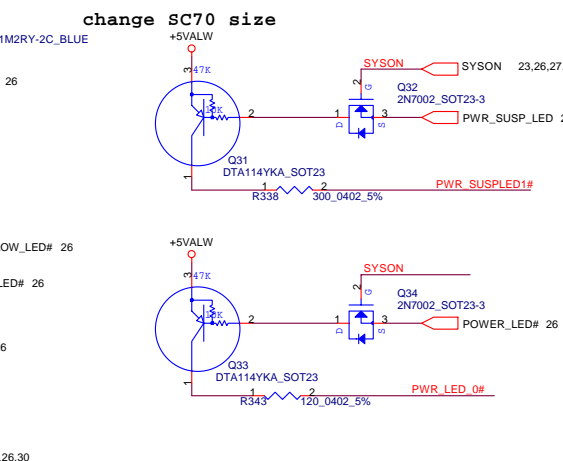
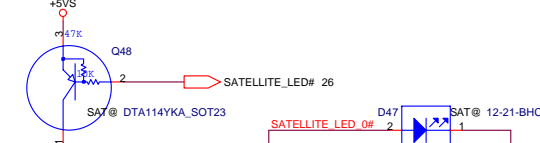
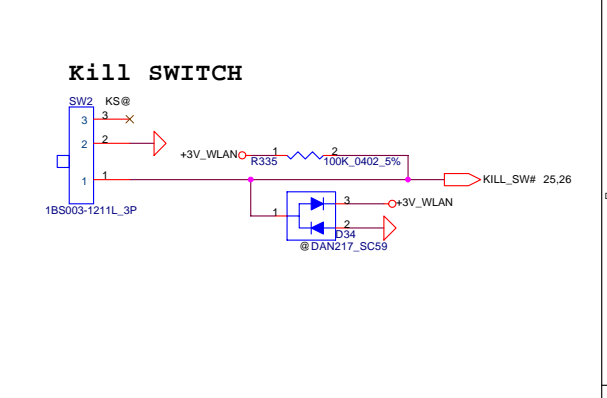
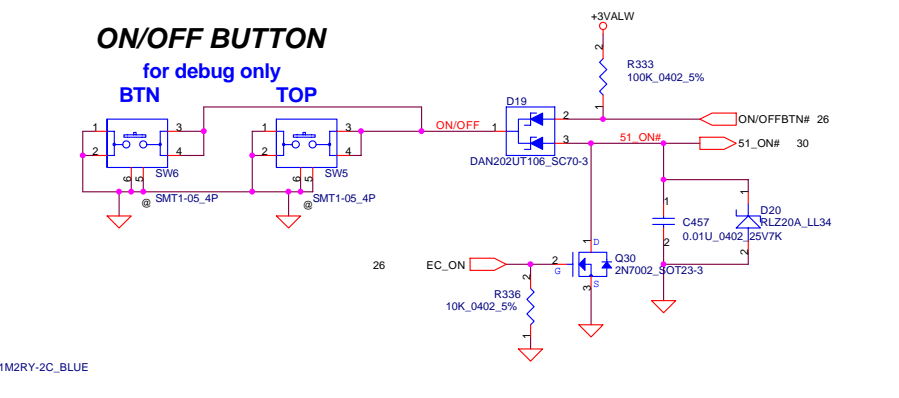
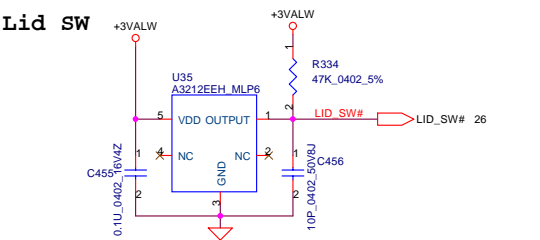
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/10/31	Deciphered Date	2009/11/13	Title	
				AMP/Volume Encoder/Audio Jack/MIC	
				Size	Document Number
				Custom	ISRAE MB LA-3711P
				Date:	Thursday, March 22, 2007
				Sheet	24 of 39
				Rev	1.0

New Card



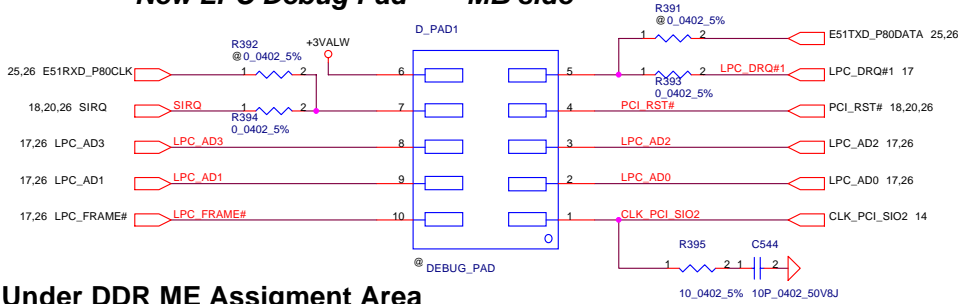
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				ISRAE MB LA-3711P	
Date:				Thursday, March 22, 2007	Sheet 27 of 39



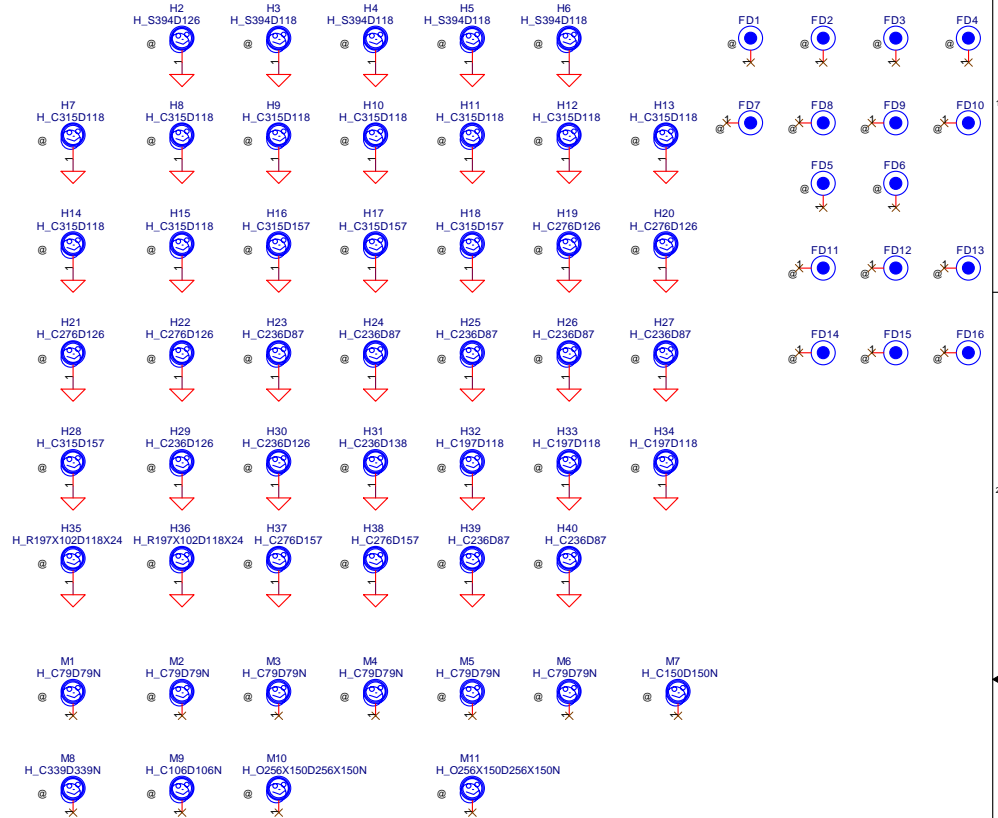
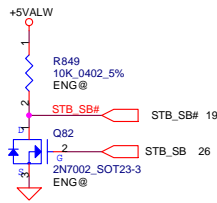
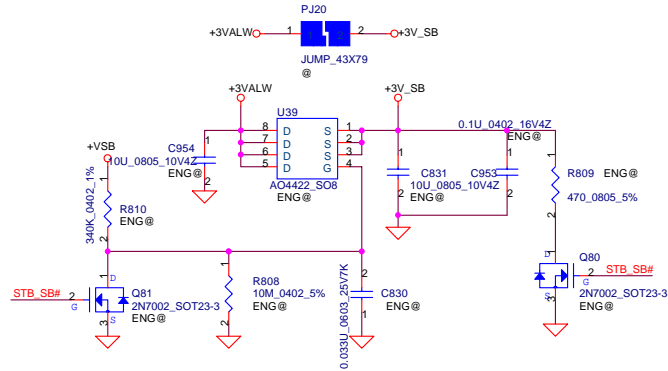
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Issued Date	2006/10/31	Deciphered Date	2009/11/13	USB/LID/KS/KB/LED/SW-B Conn
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Date:	Thursday, March 22, 2007	Sheet	28	of 39

New LPC Debug Pad ---- MB side



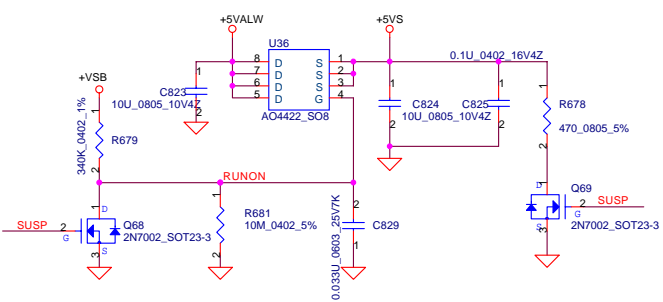
Under DDR ME Assignment Area

Keep Resistor near Debug Pad and in the same side
Reverse side DIMM ---- Pin 1 keep away DIMM

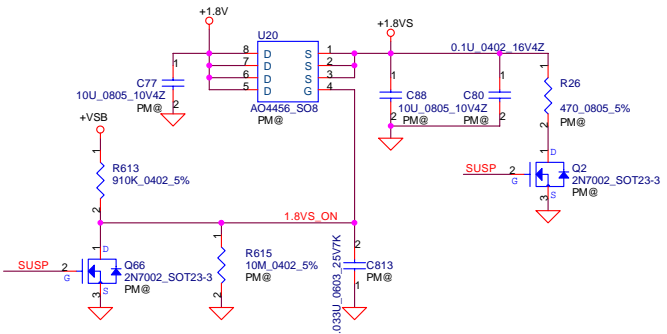


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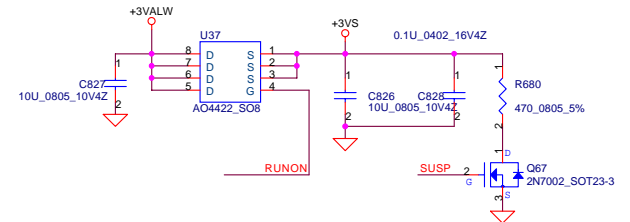
+5VALW to +5VS Transfer



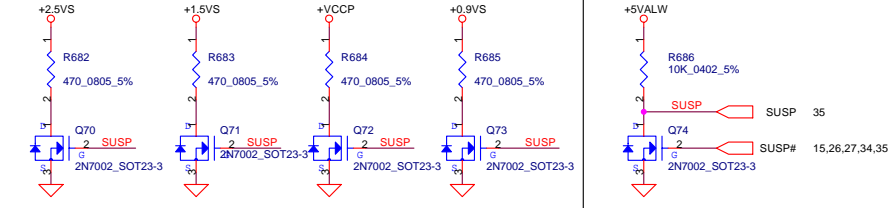
+1.8V to +1.8VS Transfer (Place close to VGA-Connector)



+3VALW to +3VS Transfer



Discharge Circuit

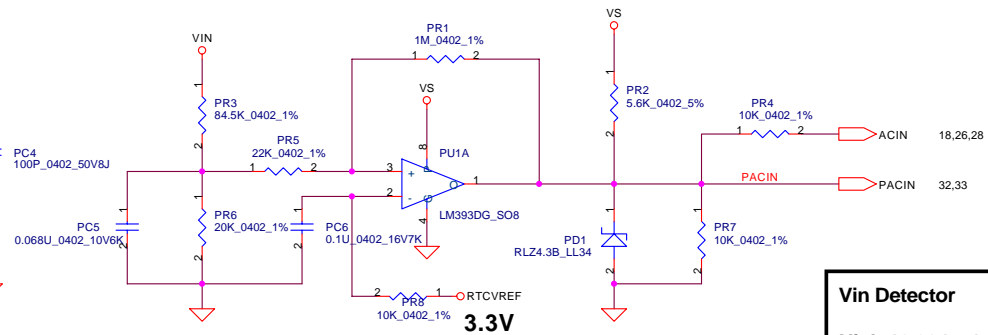
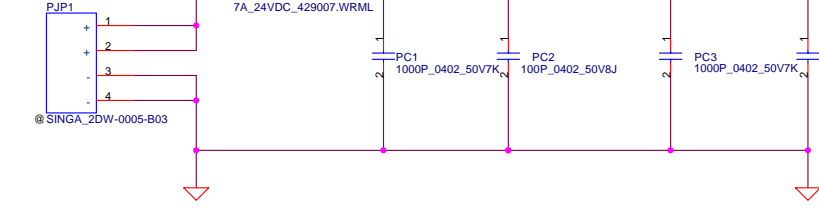


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		2009/11/13

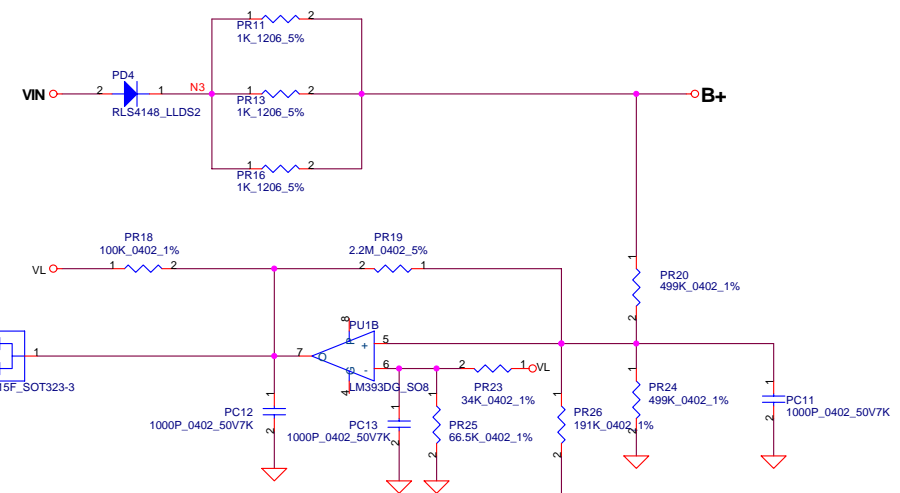
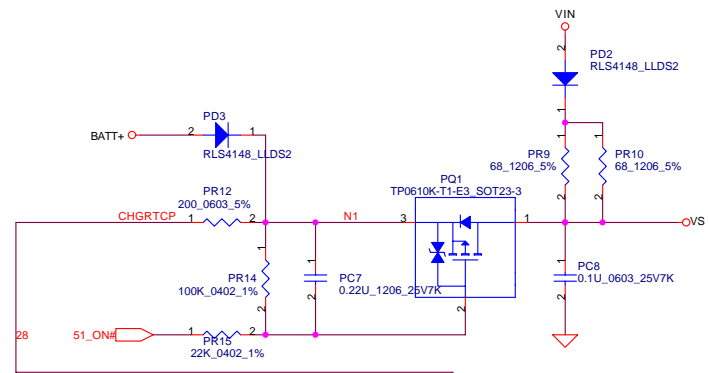
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Title		
Compal Electronics, Inc.		
DC/DC I/F Debug I/F Screw		
Size	Document Number	Rev
	ISRAE MB LA-371IP	1.0
Date:	Thursday, March 22, 2007	Sheet 29 of 39

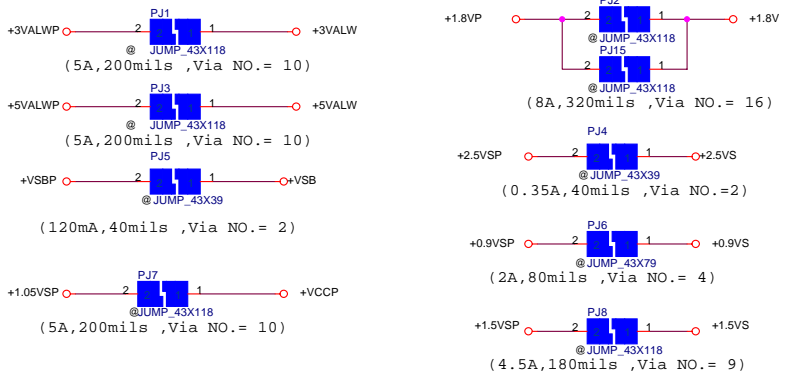
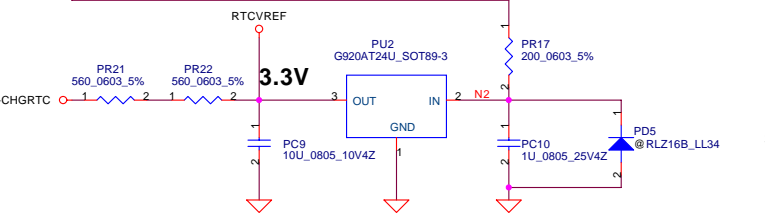
DC301001N00



Vin Detector
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



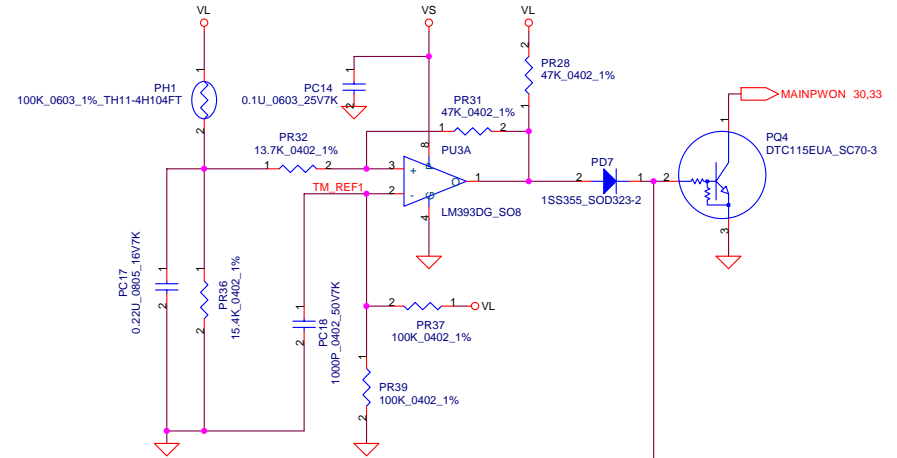
Precharge detector
15.97V/14.84V FOR
ADAPTOR



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Size	Document Number				Rev
					1.0
Date:	Thursday, March 22, 2007	Sheet	30	of	39

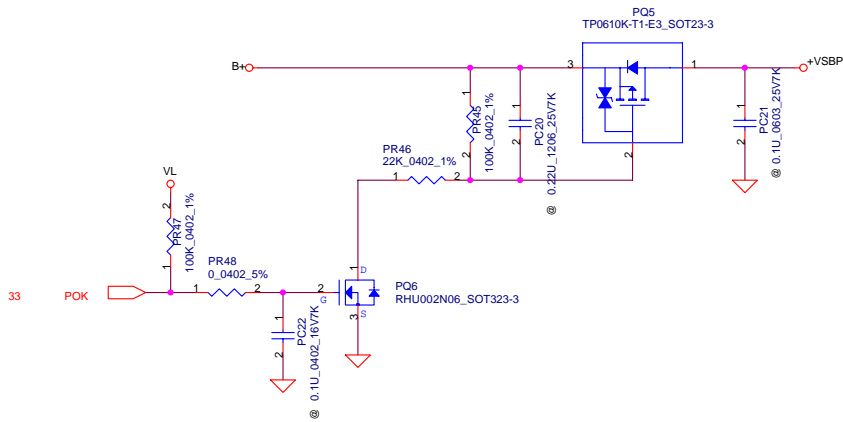
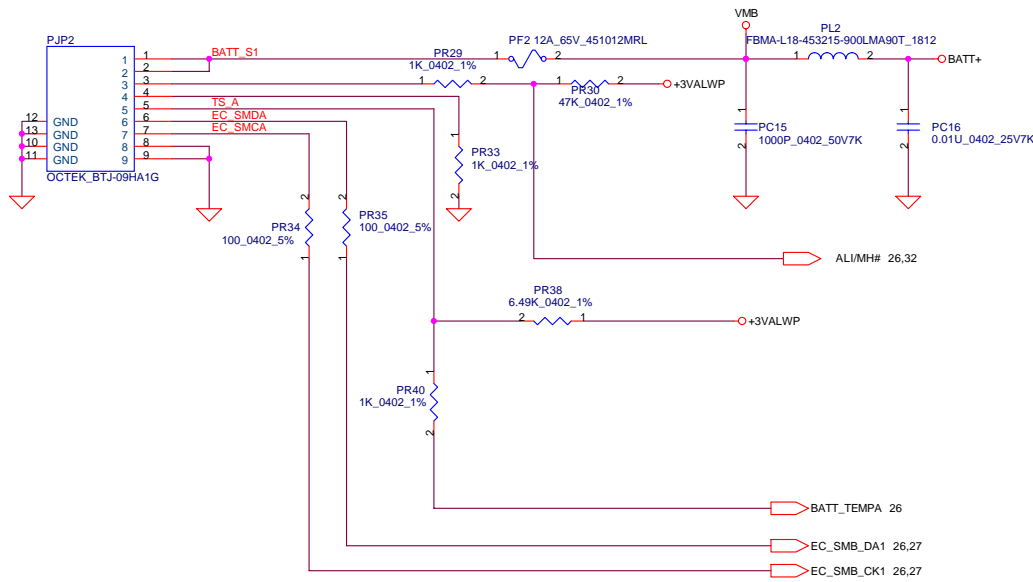
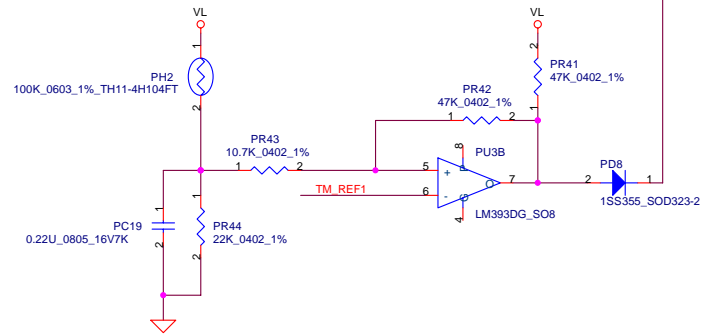
PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C

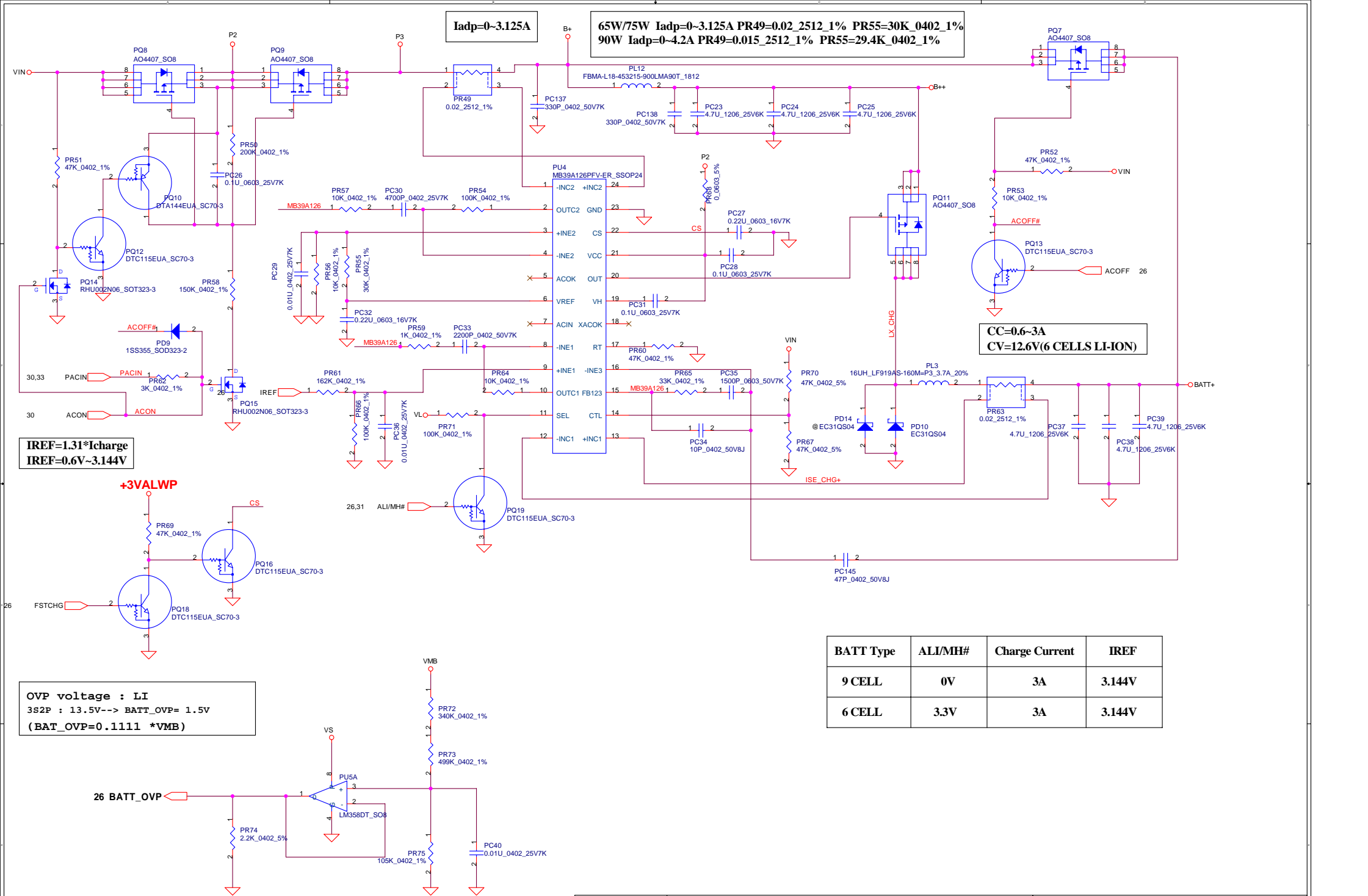


PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C
Recovery at 45 degree C



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Size	Document Number			Rev	1.0
Date:	Thursday, March 22, 2007	Sheet	31	of	39



Iadp=0~3.125A

65W/75W Iadp=0~3.125A PR49=0.02_2512_1% PR55=30K_0402_1%
 90W Iadp=0~4.2A PR49=0.015_2512_1% PR55=29.4K_0402_1%

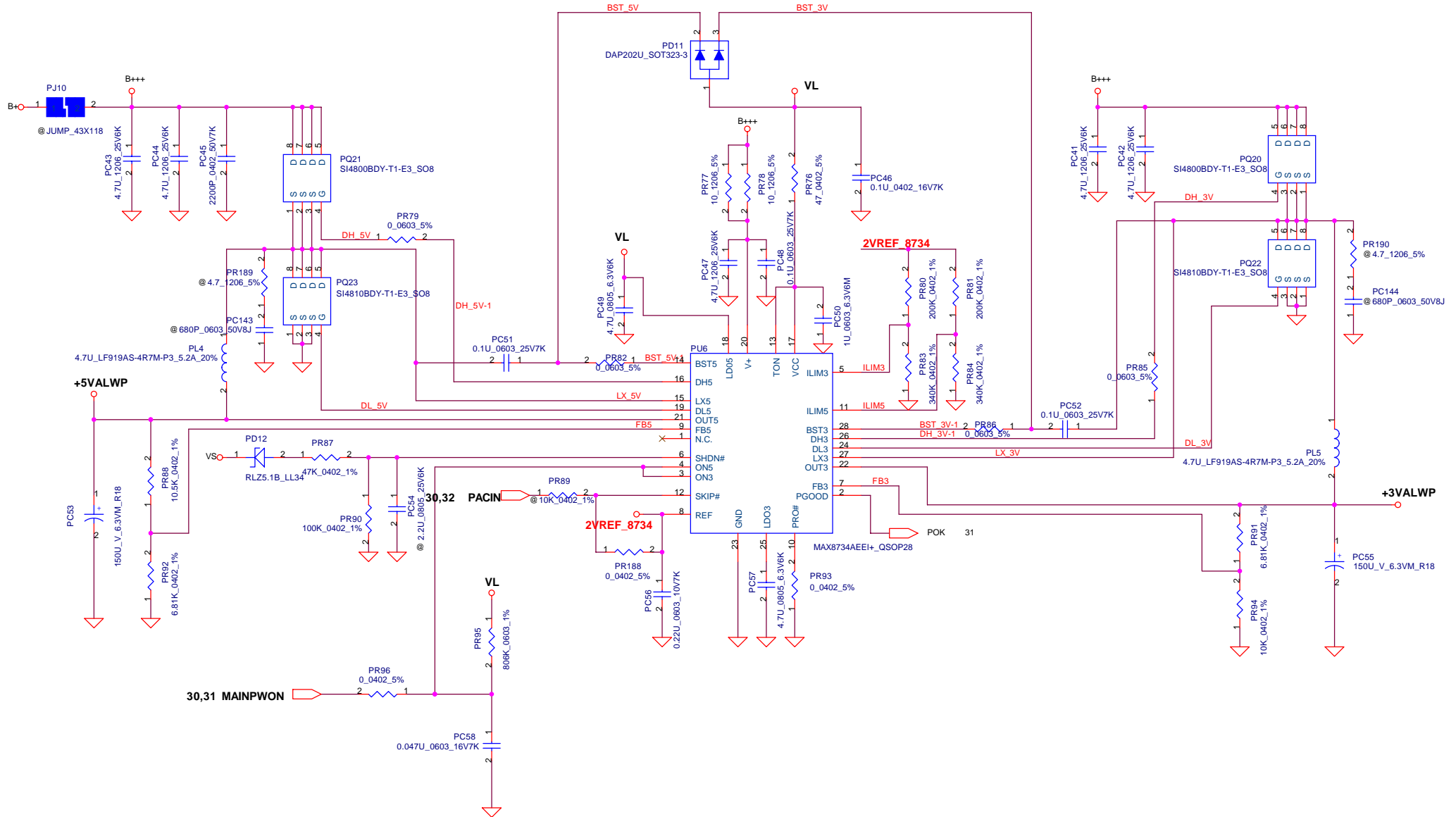
CC=0.6-3A
 CV=12.6V(6 CELLS LI-ION)

IREF=1.31*Icharge
 IREF=0.6V~3.144V

OVP voltage : LI
 3s2P : 13.5V--> BATT_OVP= 1.5V
 (BATT_OVP=0.1111 *VMB)

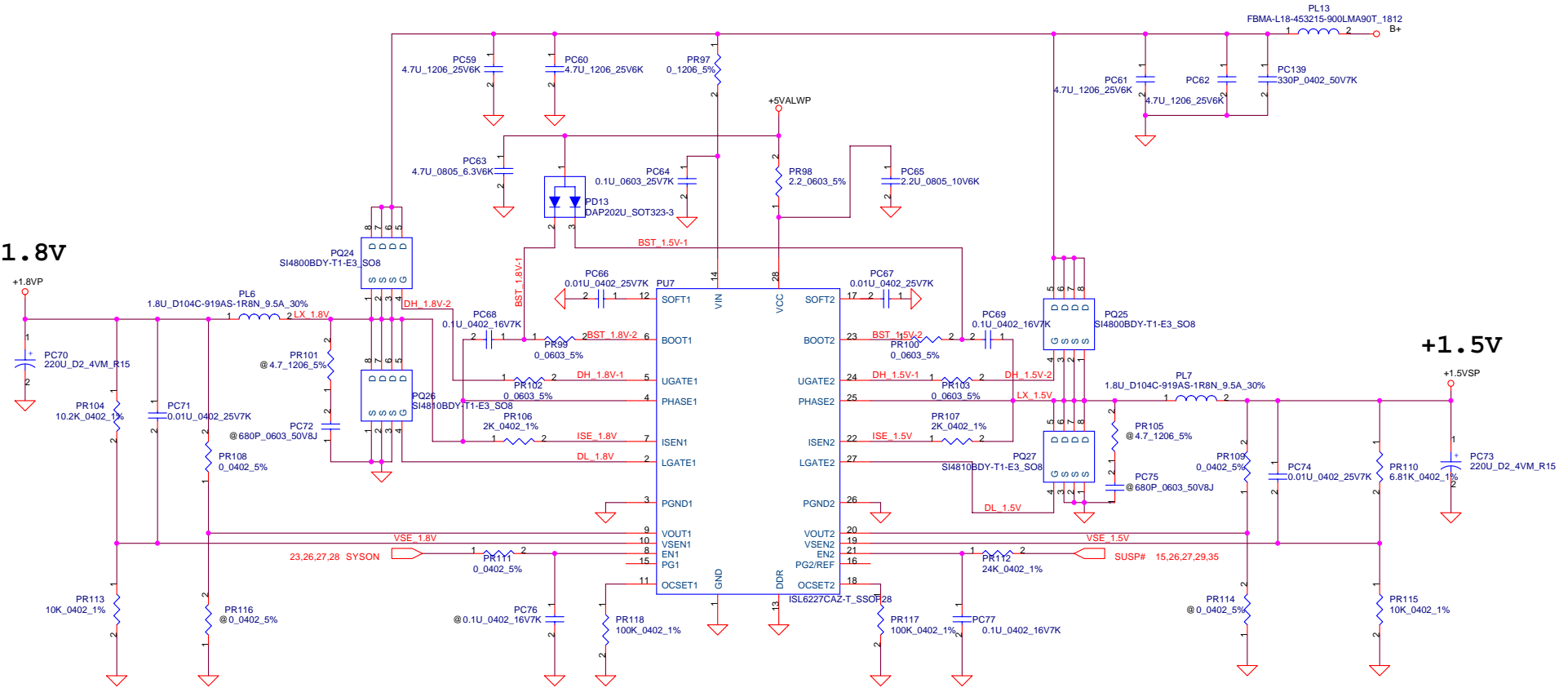
BATT Type	ALI/MH#	Charge Current	IREF
9 CELL	0V	3A	3.144V
6 CELL	3.3V	3A	3.144V

+3.3VALWP/+5VALWP



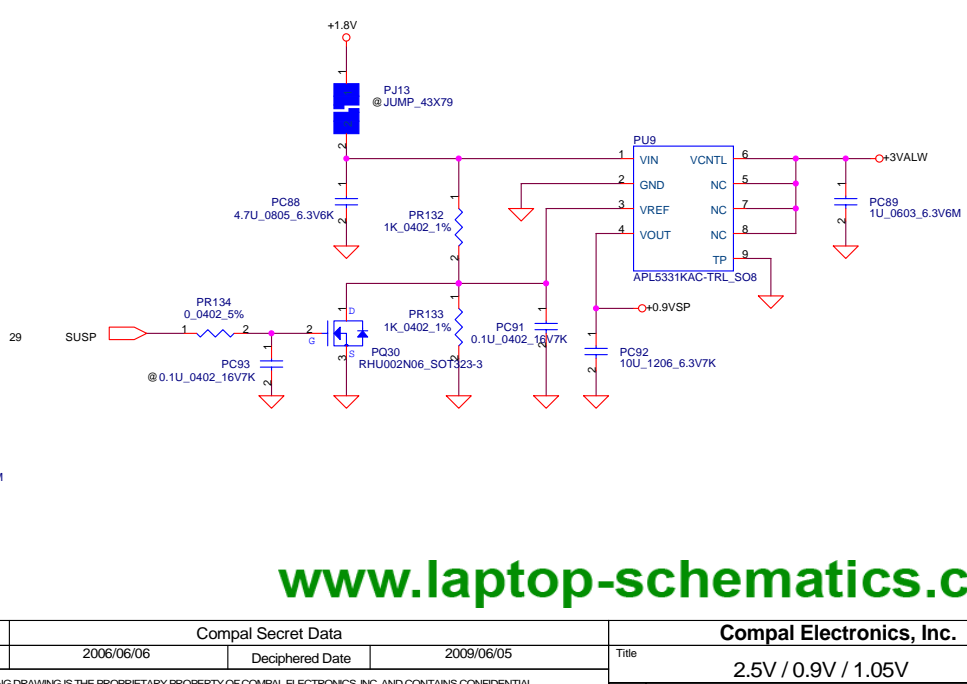
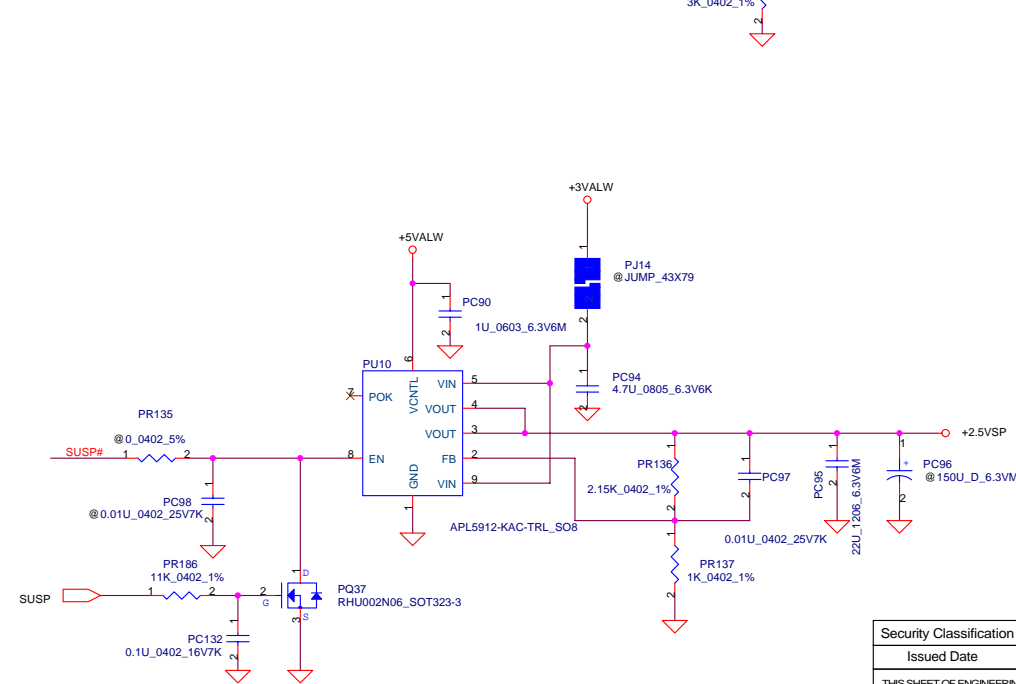
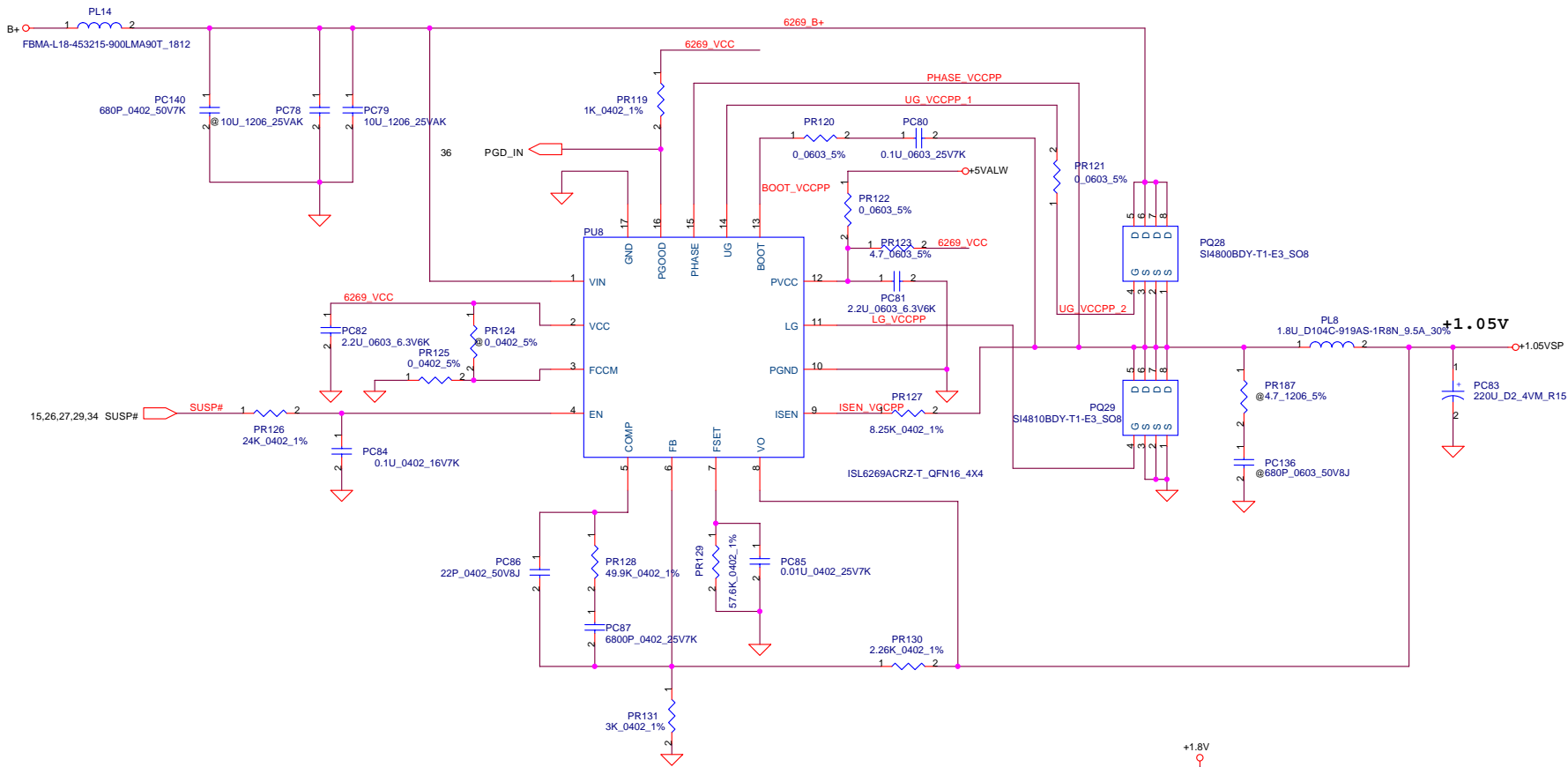
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Date:	Thursday, March 22, 2007	Sheet	33	of	39

+1.8V



+1.5V

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Size	Document Number				Rev
Date:	Thursday, March 22, 2007	Sheet	34	of	39



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Date:	Thursday, March 22, 2007	Sheet	35	of	39

HW4 Product Improvement Record (P.I.R.)

Phase: B to C		Date: 2007/01/24			Writer: Timo Teng		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
P17	Change Connector	JP24	SUYIN_06802-TK102	SUYIN_127043FB 022G345ZR_NR	Change layout footprint	0.2	
P18	Delete Component	R873 R874	100K_0402_5%	NC	All sku keep 5 in 1 and 1394 functions		
P22	Delete Component	R820	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P25	Delete Component	R195	10K_0402_5%	NC	No need more than one pull-high resistor on the net		
P26	Delete Component	Q65/Q77 R821/R822	MMBT3904/10K_0402_5%	NC	No engine start, so follow Dallas project.		
P20	Change net	R234	Connects to +3VS	Connects to +5VS	Blue LED needs to connect 5V		
P24	Modify footprint	JP14/JP15	SINGA_2SJ-S351	SINGA_2SJ-T820	For solving SMT soldering poor issue		
P25	Delete Component	U38/R503/C630	CIR/100_0805/4.7U	NC	No CIR support on spec.		
P26	Add Component	R873/2FAN_DET#	NC	10K_0402/2FAN_DET#	For separate ISRAE&ISKAE EC BIOS		
P28	Modify component	R410/R411	200_0402_5%	100_0402_5%	Emonoto-san request, the LEDs increase brigtness		
P28	Modify BOM Select	Q48/R410/R411/D47/D48	NC	SAT@	Reserve Satelliate LED BOM select		
P29	Modify R Value	R613	820K_0402_1%	910K_0402_5%	For delaying and adjusting 1.8VS power sequence		
P22	Change Value	C89, C79, C90 C68, C74, C81	0.01uF_0402	0.1uF_0402	For solving EMI noise		

Phase: C to PreMP		Date: 2007/02/02			Writer: Timo Teng		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
P18	Add Component	R874/R875	NC	@1K_0402/@100K_0402	Reserve Satellite LDE detected	1.0	
P27	Modify component	C584/C580/C587	10uF_0805_6.3V	@10uF_0805_6.3V	For Cost reduce (PVT cut-in)		
P11	Modify component	C716	330uF_D2E_2.5V	@330uF_D2E_2.5V	For Cost reduce (PVT cut-in)		
P23	Modify component	C425	4.7uF_0805_10V	@4.7uF_0805_10V	For Cost reduce (PVT cut-in)		

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				Date:	Thursday, March 22, 2007	Sheet

LAN U7
 RTL8101E
 100M@

TRANSFORMER U34
 NS892404
 100M@

PCB ZZZ1
 PCB ZKU LA-3711P REV0

Card BUS U8
 8402
 8402@

SB U2
 ICH7
 ICH7R1@

NB U6 U6
 945GM 943GML
 GMR3@ GMLR3@
 U6 U6 U6
 945GM 943GML 945PM
 GMR1@ GMLR1@ PMR1@

SKU ID R349
 18K_0402_5%
 PM@

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				Size	Document Number	Rev
				ISRAE M/B LA-3711P 1.0		
				Date:	Thursday, March 22, 2007	Sheet 38 of 39

POWER PIR LIST

page Reason for change

Modify list

DVT	35	Change +1.05V PWM IC	Change PU8 to ISL6269A(SA00000GU80), add PR122 (0ohm, SD013000080)
	36	For EMI team request to add snubber and gate resistor Modify the CUP CORE load line and compensation	Add snuber PR155,PR165(6.8ohm_SD011680B80), PC109,PC118(680p_SE024681J80) and gate resistor PR154,PR162(1ohm_SD013100B80) Change PC103 to 0.022u(SE076223K80), PC104 to 2.2u(SE107225K80), PR185 to 4.42K(SD000004J80), PC129 to 0.1u(SE076104K80, add PC126 (0.018U_SE025183J80), delete PC105 and PC106
	31	Modify the CPU OTP point from 84 degC to 87 degC for thermal team request	Change PR36 from 22K to 20K(SD034200280)
PVT	32,34, 35,36	For EMI team request to add bead to reduce board band	Add PL12,PL13,PL14(SM010020720);PC137,PC138,PC139(330p_SE074331K80);PC140(680p_SE074681K80);PC141(3300p_SE074332K80)
	33	Reduce the power consumption on S3/S4	Add PR188(0_0402_5%) and unpop PR89
	36	Solve the high frequency noise.	Change PC99 from 100U to 220U(SF22004M210)
Pre-MP	36	For EMI solution	Add PC142 (0.01u_0402)
	36	PC99 was interfere with logic low so change to small size	Change PC99 from 220U to 100U and add PC143,PC144(68U_25V).

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				Custom		1.0
Date:				Thursday, March 22, 2007	Sheet	39 of 39